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Characterization and modeling of amorphous silicon-based thin film transistor topologies for ULSI memories

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by

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DEDICATION

To my parents, Elaine and Marvin Schaefer, who have, with their faith, support, and integrity, help mold my future.

To my wife, Ann Schaefer, for her constant love and understanding.

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ABSTRACT

Hydrogenated amorphous silicon (a-Si:H) technology has been used for many years for large area displays, xerography, photovoltaics, and thin film transistors (TFTs). It has been proposed that by adding a floating gate to a TFT, a non-volatile memory cell could be fabricated. However, standard memory circuits must be re-designed to work with these devices since a-Si:H has different properties than crystalline silicon. The TFT processing steps and material attributes need to be refined to fabricate a device with proper characteristics. In addition, the material characteristics need to be incorporated into a device model for computer simulation. In this thesis, two models are considered; typical MOSFET equations and a model based upon fundamental semiconductor physics. It will be shown that the MOSFET model does not accurately simulate the TFT's behavior and in complex circuits the simulation errors quickly become unacceptable. The second model will be shown to predict the TFT's behavior with a higher degree of accuracy. The model includes other electrical properties such as the a-Si:H's density of states, dielectric properties, and the TFT's flatband voltage. Also presented are the material characteristics as well as how the materials are deposited to create a TFT in the inverted staggered structure.

1 INTRODUCTION

1.1 Project Overview

Conventional crystalline silicon wafer processing is a relatively costly manufacturing method and the fabricated circuits are of a limited size. The size is ultimately limited to the diameter of the wafer, typically 6 to 8 inches. For ultra large scale circuits, this restriction can be quite costly and confining. Roll-to-roll processing using a flexible substrate of polyimide, on the other hand, can be used to fabricate circuits on very large area substrates at a fraction of the cost of conventional wafer processing. Unfortunately, the available technology produces hydrogenated amorphous silicon (a-Si:H) which can result in some performance loss as compared to crystalline silicon. Nonetheless, a-Si:H has been used for many years in the production of photovoltaic cells. It has also been used in the process for making thin film transistor (TFT) flat panel displays. Therefore, the technology for producing a-Si:H is available and has been studied in great detail.

The topology of the TFT is similar to a MOSFET, except inverted. The inverted structure is required to reduce the number of interface states between the dielectric and semiconductor layers. It has been proposed that by adding a floating gate to the inverted TFT [1] a non-volatile memory cell could be created. Furthermore, the devices could be manufactured in a continuous roll-to-roll process. The implications of such a process are enormous. High-capacity large area memories of 10^{12} bits and other device intensive circuits could be produced. Applications for memories of such magnitude have existed for years. For example, high definition television (HDTV) uses a digital signal to construct the picture and the proposed memory could contain several hours of television. The

user could instantly start viewing the picture anywhere in the sequence, at any speed, forward, or reverse. Consider the implications in the computer market, users could save massive amounts of data and not swap out programs to clear hard drive space.

The project's main objective is to build an array of memory cells in a roll-to-roll process by using TFTs and TFTs with floating gates. The crystalline silicon memory circuits must be re-designed to work with these new devices. This ambitious project can not be accomplished in a single design iteration. The TFT processing steps and material attributes need to be refined to fabricate a device with proper characteristics. In addition, the material characteristics need to be incorporated into a device model for computer simulation. Two models worthy of consideration include the typical MOSFET device equations and a model based upon fundamental semiconductor physics. It will be shown that the MOSFET model does not accurately simulate the TFT's behavior and in complex circuits the simulation errors quickly become unacceptable. The second model will be shown to predict the TFT's behavior accurately since the model includes other electrical properties such as the a-Si:H's density of states, dielectric constant, and the TFT's flatband voltage.

1.2 Organization

Chapter 1 includes a literature review that surveys articles written about equations modeling the behaviors of the TFT and the characteristics of the materials used to create the TFT. Chapter 2 provides an in-depth explanation, both qualitatively and quantitatively, of the operation of the TFT. In addition, a comparison is made between the measured output and the predicted output for

both the MOSFET level 1 simulation equations and the model based on fundamental device equations. The model incorporates measured TFT properties shown in Chapter 3. Chapter 3 describes the method for creating the thin films and the process for fabricating the TFT. Furthermore, it describes the film characteristics as well as the process for characterizing the materials. Chapter 4 presents a brief review of the findings and presents recommendations for future work.

1.3 Literature Review

The literature review has been divided into three sub-sections. The first sub-section describes the role the TFT has played in semiconductor history and some developmental background. The second sub-section reviews journal articles that describe the physics of a-Si:H based TFTs. The sub-section does not include an in-depth review of the articles since most of the equations are thoroughly presented in Chapter 2. The third section includes other studies that outline the electrical characteristics of the materials used in the TFTs of this project.

1.3.1 Historical Review

Fifty-nine years ago, a patent was issued to Lilienfeld for the first TFT [2]. Although the materials used in the device Lilienfeld created could not possibly have worked, a year later a German scientist Heil used the correct materials, had the proper concepts, and may have actually created the first working TFT amplifier. Incredibly, this is thirteen years before the first recorded working transistor was even constructed. Bell Labs was the first to start working on the TFT after Heil, but unfortunately, did not continue their research where Heil's

experiments had completed. Later at Bell Labs, when Shockley finished his historic paper on the theory of p-n junctions, all research on the TFT was abandoned for many years.

In the late 1950's and early 1960's, research on the TFT had continued by several well-known companies, but the emergence of the MOSFET created a new competitor. Researchers at this period were interested in devices that were simple, easily manufactured, and more compact than the bipolar transistor, thus the MOSFET won and again the TFT faded into the background.

The story of the TFT does have a happy ending. In the last fifteen to twenty years it has had direct application as the pixel driver for large area flat panel displays. To this end, most recent commercial research is directed and companies have created very large area displays, 2 × 4 feet or larger, using high quality a-Si:H thin film transistors that are inexpensively produced in a continuous process [3]. This makes a-Si:H thin film transistors very attractive for applications in electronics, large area displays, xerography, imagers, and photovoltaics [2].

Throughout the years of development, there have been basically four types of thin film transistors [4]. They are defined by the order of deposition of the semiconductor layer, the gate insulation layer, the source and drain regions, and the gate electrode. Figure 1.1 shows the four different TFT topologies.

The staggered TFT structures have the source and drain contacts on one side of the semiconductor and the gate electrode on the opposite side, while the coplanar structures have all three terminals on the same side of the semiconductor film. In the inverted structures, the gate electrode, usually chrome, is the first layer deposited on the glass substrate. TFTs have been made with all four

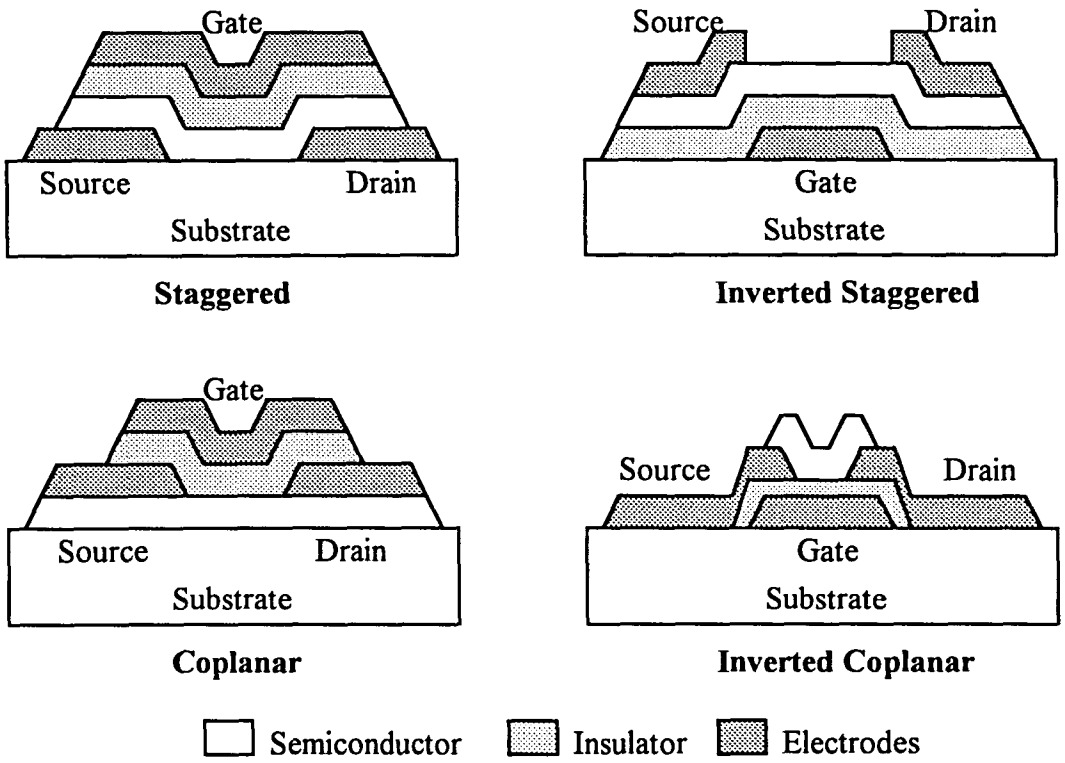

Figure 1.1. Thin film transistor topologies.

structures, but to date the topology that yields the best performance is the inverted staggered structure.

The formation of the TFT device structure involves the deposition of a-Si:H on the gate dielectric, or alternatively, deposition of the dielectric on the a-Si:H. The typical choices for the dielectric are silicon dioxide and silicon nitride grown by a plasma enhanced chemical vapor deposition (PECVD) process. Parsons et al. studied photo emissions from glow discharge deposited silicon dioxide and silicon nitride on a-Si:H and found distinctly different bonding properties at the interface as compared to a-Si:H deposited on silicon dioxide and silicon nitride [5]. Their research showed that a depletion layer exists at a-Si:H/SiO_2 interfaces with a

characteristic depth of 0.2μm. Furthermore, the results indicate that there is surface enhanced recombination resulting from the depletion layers for either a-Si:H grown on SiO_2 or SiO_2 grown on a-Si:H. For the case of Si_3N_4, the surface enhanced recombination occurs only when the Si_3N_4 is grown on the a-Si:H layer and not when a-Si:H is grown on the Si_3N_4 layer. This clearly demonstrates that silicon dioxide is unusable for high performance TFTs and for maximum results a-Si:H films should be deposited over the silicon nitride layer, not visa-versa. Therefore, the inverted structure with Si_3N_4 has been used for manufacturing high quality TFTs in industry.

1.3.2 Physics of a-Si TFTs

In 1983, M. Shur and M. Hack submitted a paper to the Physical Society of Japan entitled "A New Analytical Approach to Amorphous Silicon Thin Film Transistors" [6]. In this paper, they distinguish among three basic device operations, sub-threshold, threshold, and above threshold. In the sub-threshold regime and low gate voltages, nearly all the induced charge goes into the localized states in the interstitial defects. However, as the gate voltage increases, the Fermi level gets shifted closer to the conduction band and enters into the tail states causing mobile carriers to be introduced into the channel. This region of operation is called above-threshold. The required potential to start inducing charge into the conduction band, is referred to as threshold or the threshold gate voltage. It had been previously thought that conduction occurs through the channel only when all of the induced charge goes into the conduction band. Unfortunately, this occurs only at unrealistically high gate voltages or at electric fields that are higher than the breakdown voltage through the insulator. The theories Hack and Shur present

suggest it is actually the tail states that determine the above threshold regime currents in a-Si:H thin film transistors.

Also presented is the theory that the density of states energy spectrum can be divided into two groups: deep localized states and tail states with a transition around 0.15 eV below the bottom of the conduction band (see Figure 1.2). According to the mechanism proposed, the transition from the sub-threshold region to the above threshold region occurs when the Fermi level enters the acceptor like tail states. One explanation for this is the characteristic energy of the deep states is 1000°K and for the tail states it is 300°K. At room temperature, 300°K, and low gate voltages, all of the induced charge enters the deep states and is centered closely around the Fermi level. At high gate voltages, the Fermi level enters the tail states and at room temperature the charge has enough thermal energy to reach the conduction band. Several graphs were presented to confirm this theory.

Also suggested in the paper is the idea that in the above threshold regime

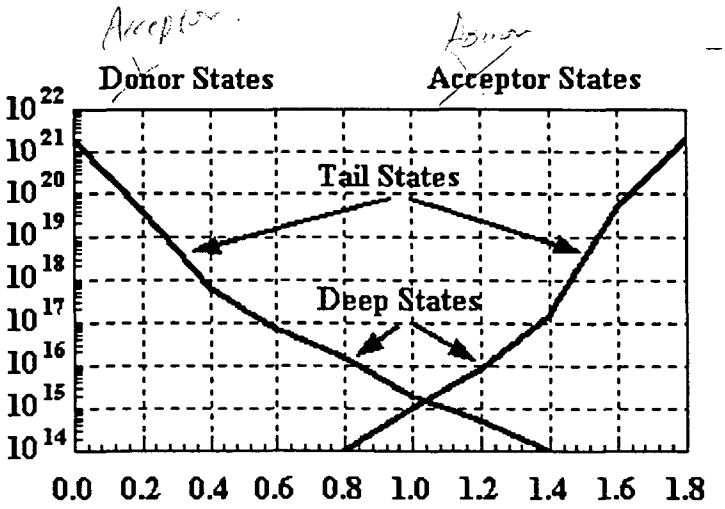

Figure 1.2. Density of states for undoped a-Si:H.

the mobility ratio, μ_{FET}/μ_{BAND}, is a complicated function of the material parameters, device temperature, and induced charge, where μ_{FET} is defined to be the field effect mobility and μ_{BAND} is the band mobility under equilibrium. The initial results of the paper suggest that the theory presented is correct.

In 1984, M. Hack and M. Shur had written a paper entitled "Physics of Amorphous Silicon Based Alloy Field-Effect Transistors" [7]. The paper discusses the density of localized states in the energy gap of a-Si:H, the charge in localized states, the field and charge distribution in the channel, the general expressions for current-voltage and capacitance-voltage characteristics of a-Si:H TFTs, the characteristics of a-Si:H TFTs below threshold, the transition to the above threshold regime, and the a-Si:H TFT characteristics above threshold. The article gives a detailed analysis of the physics of a-Si:H TFTs, deriving the equations from standard semiconductor physics. Unfortunately, the level of detail is too complex to be incorporated into a convenient and compact model.

An applicable segment of the article is the derivation of the density of states equation. As was mentioned in the previous article, the density of states for undoped a-Si:H can be broken into two categories, deep states and tail states. These states can be modeled approximately by an exponential equation. Furthermore, the conduction band states may not be constant and an exponential equation can be used as well.

In 1989, M. Hack, J. Shaw, and M. Shur had written a paper entitled "Development of Spice Models for Amorphous Silicon Thin-film Transistors" [8]. In this paper, they indicate that they have successfully incorporated a TFT device model into PSPICE by creating a three terminal TFT device. They state that this

model has significant improvements over an older version, one being the channel length shortening effect has since been taken into account.

They state in order to create a useful model in PSPICE, the currents and current derivatives at each terminal for all possible voltages must be known. Furthermore, the capacitance between each of the three terminals must be found. The results are furnished and the model seems to be in good agreement with their measured data. Furthermore, the MOSFET level 1 model is shown to be inadequate compared to their model.

In a paper entitled "An Analytic Model for Calculating Trapped Charge in Amorphous Silicon" [9], J. G. Shaw and M. Hack present a solution for calculating the charge trapped in the band states as well as how to calculate the charge available to carry current in the conduction band. In order to achieve such a task, the density of states distribution must be accurately represented and Fermi-Dirac statistics must be used since the Boltzman approximation is not always accurate. The trapped charge in the band states can be found by integrating the product of the density of states distribution functions, $g_a(E)$ for acceptor like states and $g_d(E)$ for donor like states against the Fermi-Dirac occupation function over the energy gap. Similarly, the free carriers are calculated by integrating the same function from its respective bandgap edge to infinity. One result of performing the calculations is to derive the field effect mobility as a function of the Fermi level. The ratio of free carriers to the total number of induced carriers is the ratio of field effect mobility to the band mobility.

In another article in 1989, M. Hack, M. Shur, and J. Shaw described the implementation of their model [10]. The paper starts out contrasting the performance and physics of a-Si:H to crystalline silicon. The first difference is the

carrier band mobilities in a-Si:H are two orders of magnitude lower with μ_n = 0.1 to 20 $cm^2/V \cdot s$ and μ_p = 0.05 to 10 $cm^2/V \cdot s$. Secondly, there is a continuous distribution of localized states or traps associated with dangling bonds in the bandgap of a-Si:H. The large space charge densities occur within the a-Si:H bandgap causing the carrier lifetime to be drastically reduced. It is this effect that makes it impossible to create efficient bipolar devices from a-Si:H. Furthermore, the density of states in the band gap is not symmetric; there are more donor like states then acceptor like states. This effect causes intrinsic a-Si:H to be slightly n-type. As a result, n-channel devices start with the Fermi level closer to the conduction band than p-channel devices and will be able to carry higher current densities.

The paper also shows the derivation of the equations used in their simulation program. However, the paper gives the field effect mobility in the form of a curve fit solution. This is not acceptable for this project since the density of states in the band gap most surely will be different from theirs. They also explain how channel length shortening effects can be accounted for by considering an ideal a-Si:H TFT in series with an n-i-n diode. However, the equation they use to approximate the n-i-n diode has constants that will also depend on the material and can not be found empirically.

The capacitance-voltage characteristics can be found by finding the charge in the channel, Q. The charge can be found by integrating the induced charge over the channel length. When the gate voltage is below flat band, the gate to source and gate to drain capacitances, C_{gs} and C_{gd}, are assumed to be given by the geometric overlap values, C_{gso} and C_{gdo}. When the gate voltages are above

threshold, the overall capacitances are such that $C_{gs} = C_{gsi} + C_{gso}$ and $C_{gd} = C_{gdi} + C_{gdo}$.

1.3.3 Material Characteristics

In order to accurately model TFTs, the characteristics of the dielectric and the a-Si:H need to be used. The dielectric layer could be created by using two different materials; aluminum nitride (AlN), and silicon nitride (Si_3N_4). The importance of the dielectric is to provide a good insulating layer between the gate metal and the active a-Si:H layer. Furthermore, the dielectric should have excellent capacitance properties. Therefore, the significant properties of the insulator are the dielectric constant and the resistivity.

The aluminum nitride film is grown by a reactive sputtering process. This creates a film that is c-axis vertical oriented and has a dielectric constant higher than the non-oriented film. Li Xinjiao et. al. [11] report their properties and are summarized in Table 1.1.

The silicon nitride film is grown in a plasma enhanced chemical vapor deposition system and the properties of these materials can be found in many books. Table 1.2 shows the properties of silicon dioxide and silicon nitride as found in [12].

The a-Si:H properties are highly dependent to the system in which the sample is grown. Table 1.3 shows the a-Si:H properties as given by [3].

Table 1.1. The material properties of c-axis vertical oriented aluminum nitride reported by [11].

Dielectric constant	8.8 - 10.9
Breakdown electric field	$(1.7 - 4.6)\times10^{8}$ V·m^{-1}
Resistivity	7×10^{9} to 2×10^{11} Ω·m
Refractive index n	1.9 - 2.1
Solution rate	$(20\text{-}36)\times10^{-10}$ m·s^{-1}
Thickness index b	0.2 - 2.3
Activation energy of conductivity	0.8 - 1.6 eV
Temperature Coefficient of ε	$(76\text{-}190)\times10^{-6}$ °C^{-1}

Table 1.2. The material properties of silicon nitride reported by [12].

Structure	Amorphous
Density (g/cm^3)	3.1
Refractive index	2.05
Dielectric constant	7.5
Dielectric strength (V/cm)	10^7
Infrared absorption band (μm)	11.5 - 12.0
Energy gap (ev)	~5.0
DC resistivity (Ω-cm)	~10^{14}
Etch rate in buffered HF (Å/min.)	5 - 10

Table 1.3. The material properties of a-Si:H reported by [3].

Fermi level in intrinsic material (E_c-E_{Fo}, eV)	~0.6 - 0.7
Deep localized states density at $E=E_{Fo}$ (cm^{-3} eV^{-1})	10^{15} - 10^{16}
Deep states characteristic energy (meV)	86
Tail localized states density at $E=E_c$ (cm^{-3} eV^{-1})	~2 × 10^{21}
Tail states characteristic energy (meV)	23
Width of tail states band (meV)	~ 150
Dielectric Constant	~ 11.0
Diffusion Constant	0.26-0.52 for electrons 0.13-0.26 for holes
Effective density of states in the conduction band (cm^{-3})	~ 10^{19}
Effective density of states in the valence band (cm^{-3})	~ 10^{19}
Energy gap (eV)	1.72
Index of refraction	3.32
Mobility (cm^2/V-s)	10-20 for electrons 5-10 for holes

2 MODELING THIN FILM TRANSISTORS

The project's main objective is to build an array of memory cells in a roll-to-roll process by the use of TFTs and TFTs with floating gates. The understanding and modeling of TFTs are essential to the design of such circuits. The following chapter first describes analytically the topology and operation of the TFT and presents two possible solutions to modeling a TFT. The two methods are the use of the MOSFET modeling equations to approximate the TFT, and modeling TFTs with fundamental physical device equations. Proper circuit biasing requires the key electrical properties to be known and modeled such as the a-Si:H's density of states, insulator's dielectric constant and resistivity, and the TFT's flatband voltage to name a few. These measured material properties presented in this chapter are shown without explanation since chapter 3 describes the measurements and techniques in greater detail.

2.1 Staggered Inverted TFT Topology

As was mentioned before, the TFT topology is comparable to the MOSFET topology, except the structure is inverted and the TFT materials must be deposited. Figure 2.1 shows the cross-sectional view of the MOSFET with the typical dimensional parameters. The channel is formed in the crystalline substrate by a voltage applied to the gate and the current is carried between the source and the drain. The source and drain regions are diffused into the substrate and the silicon dioxide is thermally grown from the crystalline substrate. All processing, except final metalization, is centered around the original crystalline substrate.

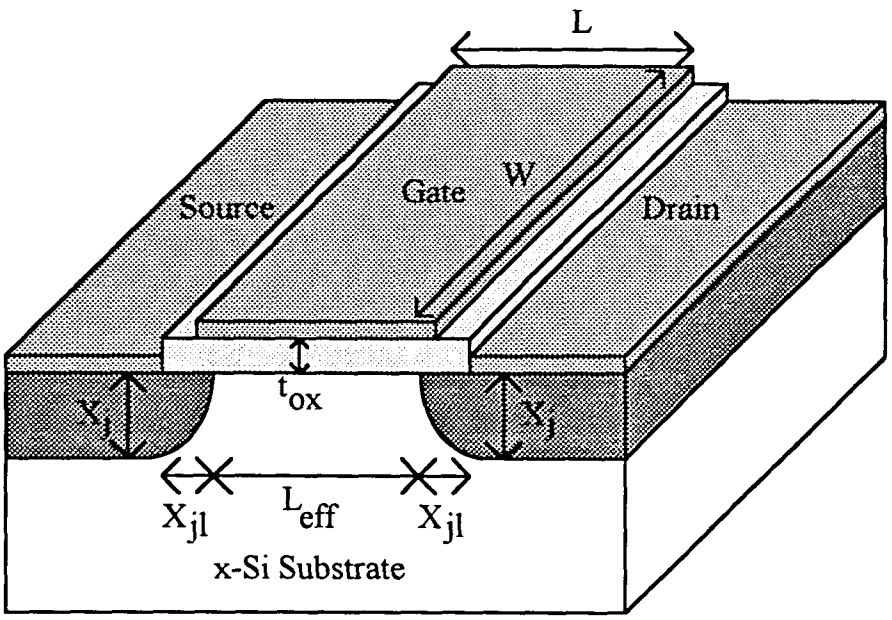

Figure 2.1. Cross-sectional view of the MOSFET with dimensional parameters.

Figure 2.2 shows the cross-sectional view of the TFT. Unlike the MOSFET, the gate is on the bottom of the device and the source and drain are on the top. This topology is referred to as staggered inverted and the device is built on a non-crystalline substrate, typically glass. The TFTs in this project will eventually be built on a flexible substrate such as polyimide. However, for initial testing purposes, the devices were built on a layer of thick PECVD grown silicon dioxide on a crystalline wafer. There are many other differences between the fabrication of the TFT and the MOSFET. For instance, all the TFT layers, except for the metal, must be grown in a chemical deposition system. Also, since the first step in the process is gate metalization, all subsequent processing steps be must be performed at fairly low processing temperatures.

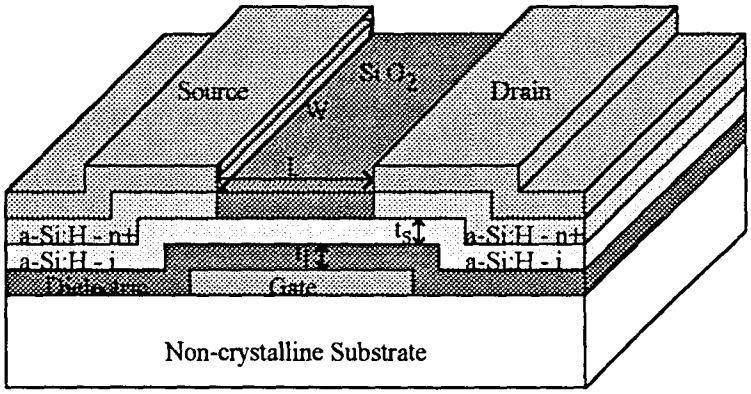

Figure 2.2. Cross-sectional view of the TFT with dimensional parameters.

2.2 TFT Basic Operations

One of the main differences between amorphous silicon and crystalline silicon is the band mobility of holes and electrons. In amorphous silicon, the band mobility is about two orders of magnitude lower. This effect will cause the device to carry much less current. The second significant difference is the continuous distribution of traps in the bandgap of amorphous silicon, as shown in Figure 2.3. From the figure, the states are not symmetrical; there are more donor like states than acceptor like states. Thus, undoped hydrogenated amorphous silicon is endowed by excess electrons or it is considered slightly n-type. It is for this reason that TFTs are created with n-channels and not p-channels.

The operation of a TFT is completely different from it's crystalline counterpart. In the below threshold region, all of the induced charge, created by applying a gate voltage slightly higher than flat band, is consumed by the deep localized states and the surface states at the amorphous silicon and dielectric interface. With more voltage applied to the gate, the deep states are filled and more and more carriers gain enough energy to fill the tail states. This causes the

Fermi level to shift into the tail states and creates an increase in mobile electrons in the conduction band. This increase raises exponentially with increasing gate voltage. The point where enough electrons are induced into the conduction band to allow significant current is know as the threshold region. In the above threshold regime, the Fermi level enters the conduction band tail states at room temperature, most of the induced charge is located well above the Fermi level and the electrons are located in the conduction band. Because of the presence of the interstitial defects, the effective mobility is much smaller than the band mobility. Two other operating regions are possible at very high gate voltages, but in normal operation these regions are not usually reached [13].

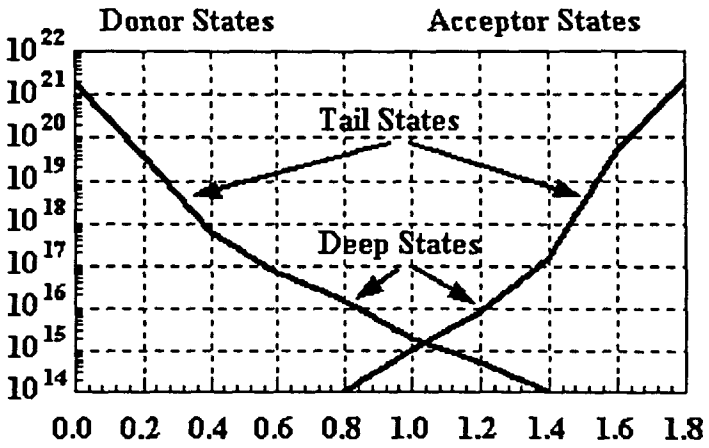

Figure 2.3. Density of states for undoped amorphous silicon.

The above discussion is based on sweeping the gate to source voltage from sub-threshold to above threshold. By sweeping the drain to source voltage when the gate to source voltage is above threshold, three different zones are encountered. Generally, the drain voltage creates an electric field between the drain and source that pushes the electrons through the channel. Ideally all the

applied voltage is used to create this current, however, the i-n+ junctions form a diode and consumes some of the potential. On the source side, the diode is in the forward active region and the loss is not significant. On the drain side, the diode is in the reverse region and must be broken down before current can be pushed through it. The breakdown voltage of the diode is referred to as the ON voltage of the TFT.

The first zone is encountered at low drain to source voltages, $V_{DS} < V_{ON}$. In this region, the diode causes drain to source current to be negligible. The second zone, the linear region, is encountered when $V_{DS} > V_{ON}$ but small enough not to push more electrons through the device than possible. The last zone, saturation, is found at high drain voltages and the electric field can not push any more electrons through the channel due to its finite thickness.

2.3 Modeling the TFT with MOSFET Equations

The modeling equations and techniques in SPICE have been an industry standard for many years. Because of its popularity and ease of use, it is relevant to model the TFT and TFT circuits using the MOSFET modeling equations. Although the MOSFET level 1 model is simplistic, it can be used to predict the behavior of TFT in limited regions. The derivations for the modeling equations can be found in a SPICE reference book [14,15] or most circuit books. It should be noted that the equations represent n-channel devices only.

In the below threshold regime the gate to source voltage, V_{GS}, is lower than the threshold voltage, V_{TH}, and the resultant drain to source current, I_{DS}, is negligible, therefore in this region

$$I_{DS} = 0 \cdot \text{Amps}. \qquad 2.1$$

In the linear regime, $V_{GS} > V_{DS} - V_{ON} + V_{TH}$, the effective drain to source voltage, V_{DS}-V_{ON}, is not large enough to saturate the channel and the current resembles a resistor. Equation 2.2 shows the drain to source current for this region.

$$I_{DS} = KP\frac{W}{L-2X_{jl}}\left(V_{GS} - V_{TH} - \frac{V_{DS} - V_{ON}}{2}\right)V_{DS}\left(1+\lambda(V_{DS} - V_{ON})\right) \qquad 2.2$$

W is the channel width, L is the channel length, X_{jl} is the lateral junction of the diffusion area, λ is the channel length modulation, V_{ON} is the drain to source voltage required to break down the i-n+ diode, and KP is the transconductance parameter which is defined as

$$KP = \mu_n \cdot \frac{\varepsilon_i \cdot \varepsilon_o}{t_i}. \qquad 2.3$$

Where μ_n is the electron mobility, ε_i is the dielectric constant, ε_o is the permittivity of free space, and t_i is the thickness of the insulator. The last mode of operation is the saturation regime, $V_{TH} < V_{GS} < V_{DS} - V_{ON} + V_{TH}$. In this mode, the drain to source voltage causes the channel to saturate and subsequent increments in drain to source voltage does not increase the corresponding current. Equation 2.4 models this regime.

$$I_{DS} = \frac{KP}{2}\frac{W}{L-2X_{jl}}(V_{GS} - V_{TH})^2\left(1+\lambda(V_{DS} - V_{ON})\right) \qquad 2.4$$

Using Equations 2.1 through 2.4 a Mathcad™ file was created to compare the MOSFET level 1 equations with the measured data from a typical TFT. The

program is presented in Appendix B. The device parameters used by the equations are shown in Table 2.1.

The parameters shown in Table 2.1 were found by forcing the modeled data to fit the measured data for the I_{DS} versus V_{GS} plot. The corresponding data for the measured TFT and the MOSFET equations are shown in Figure 2.4. Since the parameters were fitted around the measured data, the model predicts the current with some degree of accuracy at lower gate voltages. However, as the curve shows, higher gate voltages increase the percentage of error.

Figure 2.5 shows a plot of I_{ds} versus V_{ds} and shows at higher gate voltages the model quickly becomes unacceptable. The mobility could be raised to model the higher gate voltages, but at a price of losing the accuracy of the drain to source current at lower gate voltages. The reason the model does not accurately

Table 2.1. MOSFET level 1 parameters used in calculations.

Gate Width (W)	100 μm
Gate Length (L)	10 μm
Diffusion/Oxide Overlap (X_{jl})	2.5 μm
Dielectric Thickness (t_i)	500 Å
Dielectric Constant (ε_i)	5.4
Threshold Voltage (V_{TH})	5.6 Volts
ON Voltage (V_{ON})	3.0 Volts
Channel Length Modulation (λ)	0.025 $Volts^{-1}$
Electron Mobility (μ_n)	0.00011 $cm^2/Volt \cdot sec$

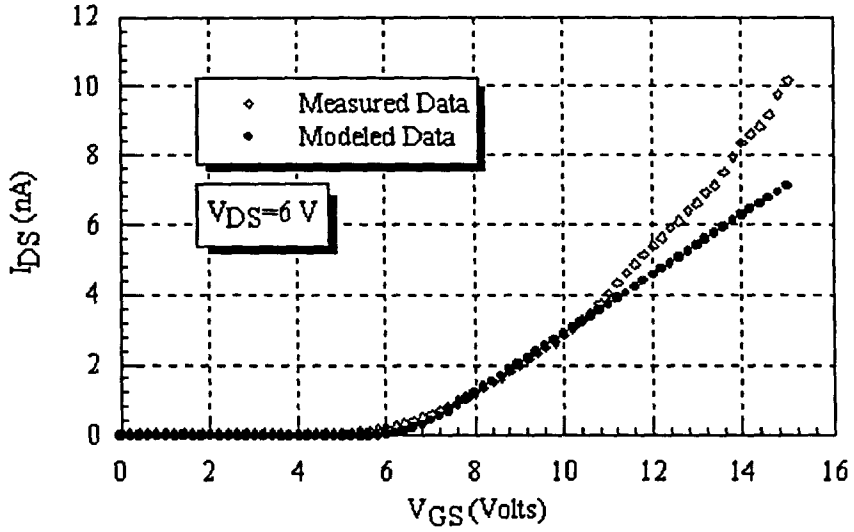

Figure 2.4. Drain to source current as a function of gate voltage for a typical TFT and the MOSFET level 1 model.

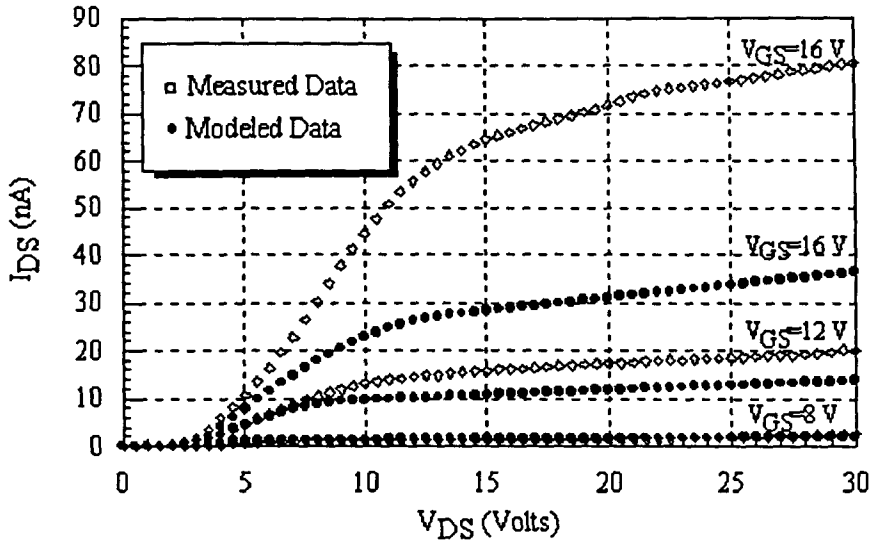

Figure 2.5. Drain to source current as a function of drain voltage for a typical TFT and the MOSFET level 1 model.

predict the current is that the equations assume all the induced charge in the channel is available for conduction. The model also does not take into account the defect density in the bandgap.

2.4 Modeling the TFT with Fundamental Device Equations

The first step is to relate the drain to source current, I_{ds}, to the gate to source voltage, V_{gs}, and the drain to source voltage, V_{ds}. It can be shown that the drain to source current is associated to the electric field along the channel as

$$I_{ds} = -q \cdot \mu_{BAND} \cdot n \cdot W \cdot F. \qquad 2.5$$

Where q is the charge of an electron, μ_{BAND} is the electron band mobility, n is the free electron concentration, W is the gate width, and F is the electric field along the channel. The electric field is defined in Equation 2.6 as

$$F = -\frac{dV}{dy}. \qquad 2.6$$

Where V is the potential across the channel and y is the direction parallel with the channel. The electron concentration in the channel can be found by utilizing the gradual channel approximation. The induced charge density in the channel per unit area is related to the induced charge at the source by

$$n_{ind} = n_{inds} - \frac{\varepsilon_i \cdot V}{q \cdot d_i} \cdot b = n_{inds} - \frac{C_{ox} \cdot V}{q} \cdot b. \qquad 2.7$$

Where n_{inds} is the charge density at the source, ε_i is the permittivity of the dielectric, V is the potential across the channel, d_i is the thickness of the dielectric,

and b is a saturation non-ideality factor. C_{ox} is the capacitance of the dielectric per unit area and can be used in place of ε_i/d_i. The drain to source voltage ideally creates an electric field of $\varepsilon_i \cdot (V_{ds}-V_{ON})/d_i \cdot q$, across the channel, however, the drain and source are not located directly across from one another and a correction factor is required. The field effect mobility can be defined as the ratio of electrons available to carry current to the induced electrons multiplied by the band mobility. This ratio is shown in Equation 2.8 as

$$\mu_{FET} = \frac{n}{n_{ind}} \cdot \mu_{BAND}, \qquad 2.8$$

where μ_{BAND} is the band mobility, and n_{ind} is the induced charge. The number of electrons available to carry current is much smaller than number induced in the channel by the electric field. Therefore, it is expected that the ratio of μ_{FET}/μ_{BAND} is small. Furthermore, the field effect mobility is a function of gate voltage since it is a function of the induced charge density. The drain to source current, I_{ds}, can be obtained by substituting Equations 2.6 and 2.8 into Equation 2.5 and integrating y across the gate length L on the left hand side and integrating V from 0 to the applied drain to source potential on the right hand side. The resultant equation is shown in Equation 2.9.

$$I_{ds} = q \cdot \left(\frac{W}{L}\right) \cdot \int_0^{V_{ds}-V_{ON}} n_{ind} \cdot \mu_{FET}(n_{ind}) \cdot dV \qquad 2.9$$

Where μ_{FET} is a function of n_{ind} and will be solved for later in the section. By using Equation 2.7 without the correction factor as a change of variables, Equation 2.9 can be rewritten as

$$I_{ds} = \frac{q}{C_{ox}} \cdot \left(\frac{W}{L}\right) \cdot \int_{n_{indd}}^{n_{inds}} n_{ind} \cdot \mu_{FET}(n_{ind}) \cdot dn_{ind}, \qquad 2.10$$

where n_{inds} is the induced charge at the source and n_{indd} is the induced charge at the drain which can be defined as

$$n_{inds} = \frac{C_{ox}}{q} \cdot \left(V_{gs} - V_{FB}\right) \text{ and} \qquad 2.11$$

$$n_{indd} = n_{inds} - \frac{C_{ox} \cdot \left(V_{ds} - V_{ON}\right) \cdot b}{q}, \qquad 2.12$$

where V_{FB} is the flatband voltage. Some amount of care needs to be used when using Equation 2.12, when $C_{ox} \cdot (V_{ds}-V_{ON}) \cdot b/q$ becomes larger than n_{inds}, n_{indd} must be set to zero and not allowed to become negative.

Equation 2.11 is only used as a first order approximation since the induced charge is shared between the conduction band and inter-gap defects. In order to find the correct induced charge at the source, the electric field profile must be found. The distribution of the electric field in the direction perpendicular to the channel for zero drain to source voltage is obtained from the solution to Poisson's equation:

$$\frac{dF}{dy} = \frac{\rho(E_f)}{\varepsilon_s \cdot \varepsilon_o}, \qquad 2.13$$

where F is the electric field in the channel perpendicular to the interface, y is the direction perpendicular to the interface, and ε_S is the dielectric constant for a-Si:H. The space charge density, ρ, can be found as a function of the Fermi level as

$$\rho(E_f) = -q \cdot \left(n_t(E_f) + n(E_f)\right), \qquad 2.14$$

where n_t is the concentration of localized charge and n is the concentration of electrons in the conduction band. The trapped charge and the free electrons can be calculated as a function of the Fermi level by integrating the density of states (DOS) distribution against the Fermi occupation function which describes the probability of occupation of a trapping center by an electron:

$$n_t(E_f) = \int_{E_c}^{E_c} g_a(E) f(E, E_f) dE, \text{ and} \qquad 2.15$$

$$n(E_f) = \int_{E_c}^{\infty} g_c(E) f(E, E_f) dE. \qquad 2.16$$

Where $g_a(E)$ and $g_c(E)$ is the density of states distribution for intrinsic amorphous silicon and the equilibrium Fermi-Dirac occupation function is defined by

$$f(E, E_f) = \frac{1}{1 + e^{\frac{E - E_f}{kT}}}. \qquad 2.17$$

To model the density of states for n channel TFTs, the acceptor like states and the Fermi level must be known. The density of states for typical a-Si:H is shown in Figure 2.3. The deep states and tail states for the acceptor like states can be approximately modeled by the exponential function

$$g_A(E) = g_1 \cdot \exp\left(\frac{E}{E_1}\right) + g_2 \cdot \exp\left(\frac{E}{E_2}\right). \qquad 2.18$$

Where g_1 and g_2 have units of $cm^{-3} \cdot ev^{-1}$ and E_1 and E_2 have units of energy in electron volts. The conduction band can be modeled in a similar manner:

$$g_C(E) = g \cdot \exp\left(\frac{E}{E_C}\right). \qquad 2.19$$

The only restriction on Equations 2.18 and 2.19 is they must be continuous at the conduction band edge. The modeled density of states is shown in Figure 2.6. It was obtained by adjusting the model until the model accurately predicted the TFTs drain to source current. The trapped charge and free electrons are shown in Figure 2.7 as a function of the Fermi energy.

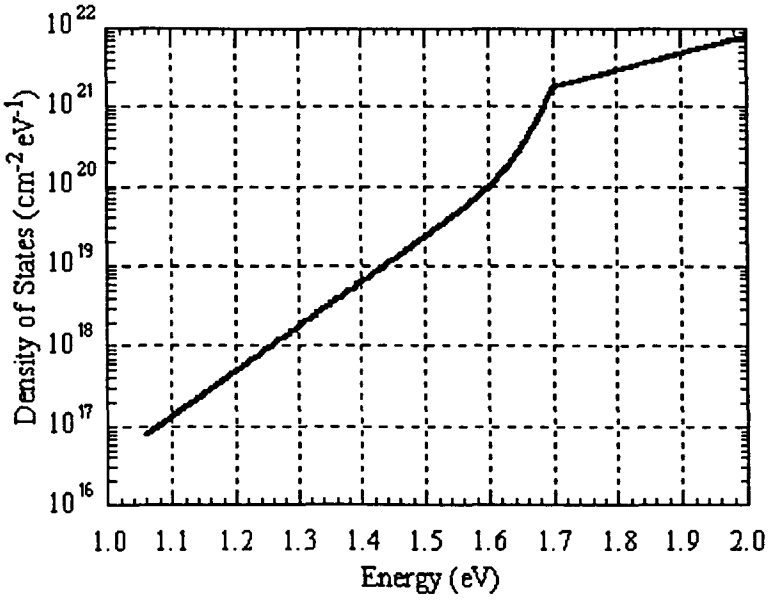

Figure 2.6. Modeled density of states for a-Si:H.

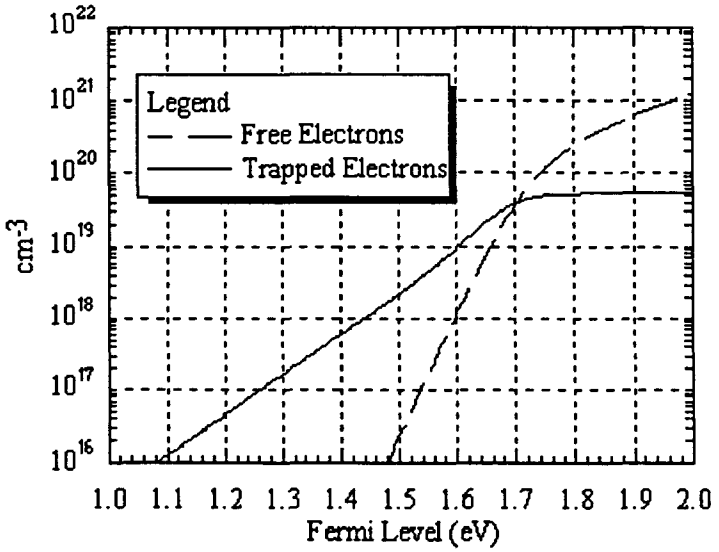

Figure 2.7. Modeled concentration of trapped charge and free electrons.

Using Poisson's equation and the relationship,

$$F = -\frac{dV}{dy}, \qquad 2.20$$

the electric field can be solved for by substituting Equation 2.20 into 2.13 and integrating V from 0 in the bulk to the potential, V_S, at the dielectric/a-Si:H interface. Equation 2.21 shows this result as

$$F = \left[\frac{2}{\varepsilon_s \cdot \varepsilon_o} \cdot \left|\int_0^{V_s} \rho(V)dV\right|\right]^{1/2}. \qquad 2.21$$

The space charge density is defined as a function of the Fermi level, thus by using the relationship q·V=E, the equation can be rewritten as

$$F = \left[\frac{2}{\varepsilon_s \cdot \varepsilon_o \cdot q} \cdot \left| \int_{E_i}^{E_i + qV_s} \rho(E) dE \right| \right]^{1/2}. \qquad 2.22$$

The electric field as a function of the band bending potential V_S is shown in Figure 2.8.

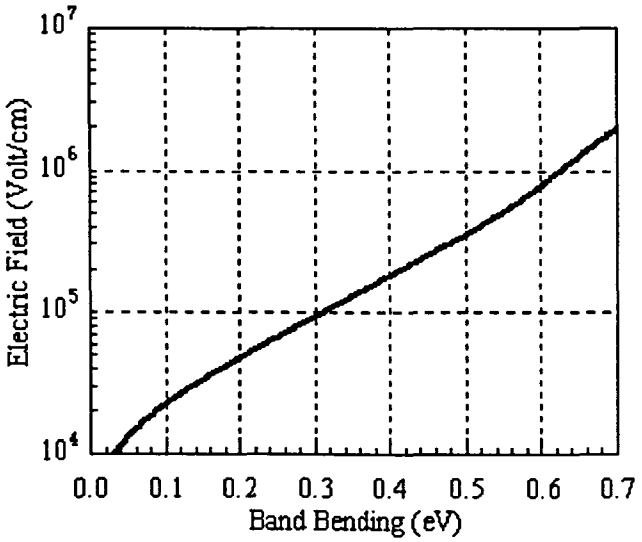

Figure 2.8. The electric field as a function of band bending potential.

The induced charge at the source, n_{inds}, as a function of the interface potential is found by

$$n_{inds}(V_s) = \frac{\varepsilon_s \cdot \varepsilon_o \cdot F_s(V_s)}{q}. \qquad 2.23$$

The electrons in the conduction band can be found by integrating the ratio of free electrons to the electric field over the channel potential as shown by

$$n_s = \frac{1}{q} \cdot \int_{E_i}^{E_i+qV_s} \frac{n(E)}{F\left(\frac{E-E_i}{q}\right)} dE. \qquad 2.24$$

Using the numerical data from Equations 2.23 and 2.24, the mobility as a function of the induced charge can be found as

$$\mu_{FET}(n_{ind}) = \frac{n_s}{n_{ind}} \cdot \mu_{BAND}. \qquad 2.25$$

Figure 2.9 shows the field effect mobility as a function of the induced charge.

The only thing left to find is the voltage at the interface as a function of the gate to source voltage. Figure 2.10 shows the band diagram and how the gate potential is related to V_S. It is assumed in the figure there is zero drain to source voltage.

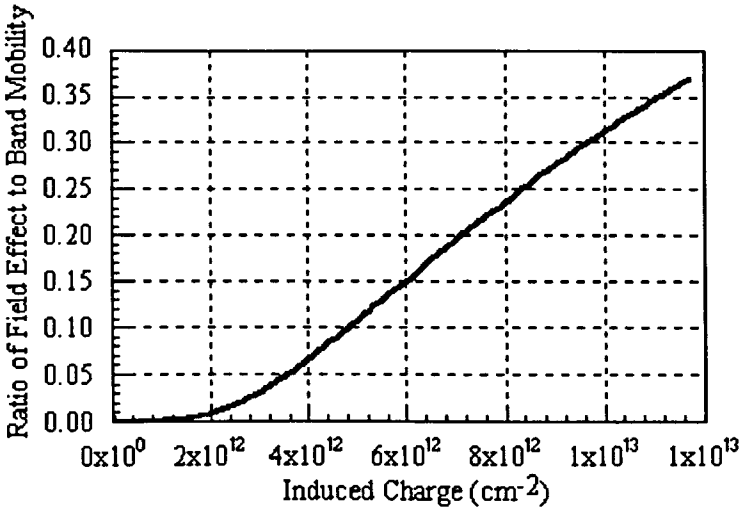

Figure 2.9. Ratio of field effect mobility to the band mobility as a function of the total induced charge.

The equation that relates the interface potential to the gate voltage is

$$V_{gs} - V_{FB} = V_s + \frac{\varepsilon_s \cdot F_s \cdot d_i}{\varepsilon_i}. \qquad 2.26$$

Using Equation 2.26 in conjunction with Equations 2.24 and 2.25 the induced charge at the surface and the field effect mobility can be found as a function of the gate voltage. Figure 2.11 shows the induced charge at the surface as a function of the gate voltage. Figure 2.12 shows the field effect mobility as a function of the gate voltage. Both graphs are valid only at the source where there is no electric field due to the drain to source voltage.

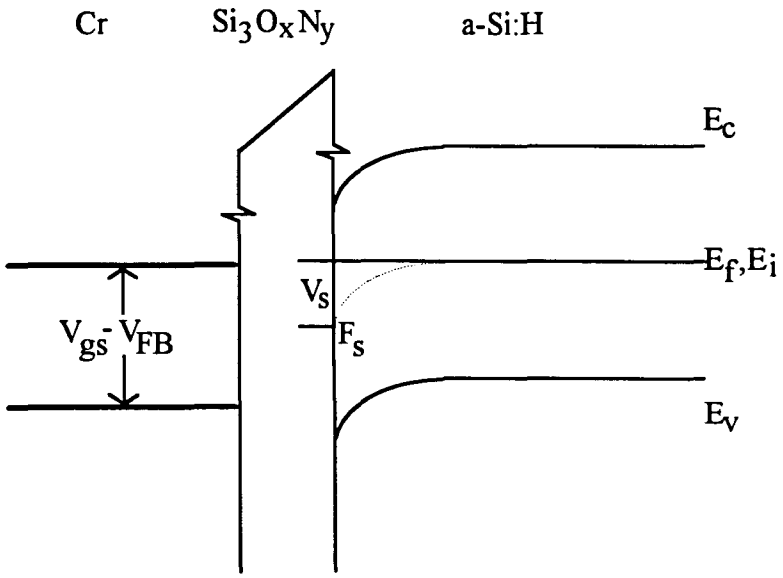

Figure 2.10. Band diagram for zero drain to source voltage.

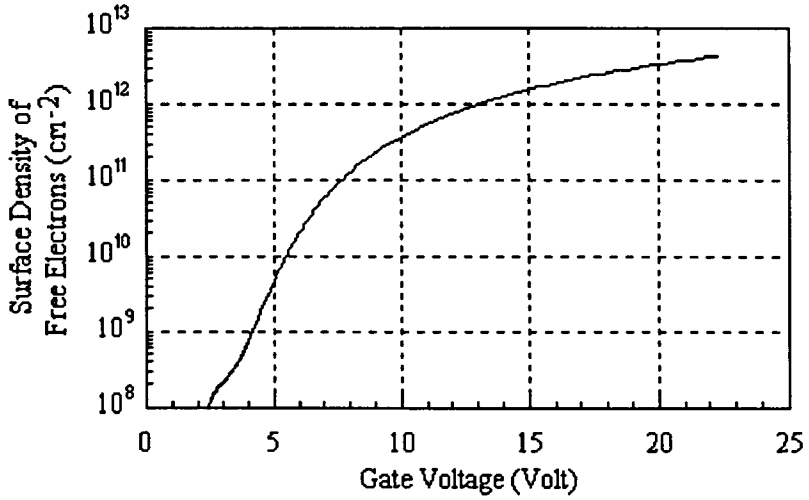

Figure 2.11. Induced charge at the surface.

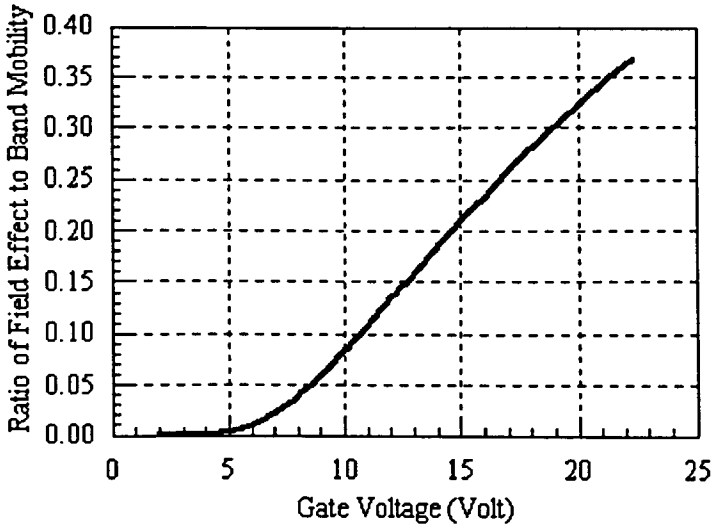

Figure 2.12. Field effect mobility versus the gate voltage.

Equation 2.10 defines the current in terms of dimensional parameters, the source and drain voltage, the field effect mobility as a function of the induced charge, and the concentration of the induced charge at the source and drain. The induced charge at the source can be found as a function of the gate to source voltage by utilizing Equations 2.23 and 2.26. The field effect mobility as a

function of the induced charge can be found by using Equations 2.24, 2.25, and 2.26 where the gate voltage must also be given. Using the aforementioned equations, a Mathcad™ file was created and it is presented in Appendix C. The TFTs were measured and the computer simulation parameters were changed to match the measured results. A list of the material parameters used in the program is shown in Table 2.2.

Table 2.2. Material parameters used in modeling a TFT.

Gate Width	100μm
Gate Length	5μm
Temperature	300°K
Dielectric Thickness	0.05μm
Dielectric Constant	5.4
a-Si:H Dielectric Constant	11.0
a-Si:H Energy Gap	1.7 eV
Intrinsic Fermi-Level	1.06 eV
Band Mobility	0.0026 cm^2/volt·sec
Deep States	$N_a = 1 \times 10^{11}$ cm^{-3}/eV $E_a = 7.8 \times 10^{-2}$ eV
Tail States	$N_a = 1 \times 10^{14}$ cm^{-3}/eV $E_a = 2.1 \times 10^{-2}$ eV
Conduction Band States	$E_a = 2 \times 10^{-1}$ eV
Flat Band Voltage	2.0 Volts
On Voltage	4.3 Volts
Saturation Voltage Correction Factor	0.8
Channel Length Modulation	0.025 $Volt^{-1}$

Figure 2.13 shows the measured data and the modeled data for a typical I_{ds} versus Vgs plot. The drain to source voltage was kept at 6 volts in order to keep the device in the linear regime. The figure shows the model predicts the behavior reasonable well, but not exactly. An obvious reason for this discrepancy is that the i-n+ diode at the source and drain was not included in the model.

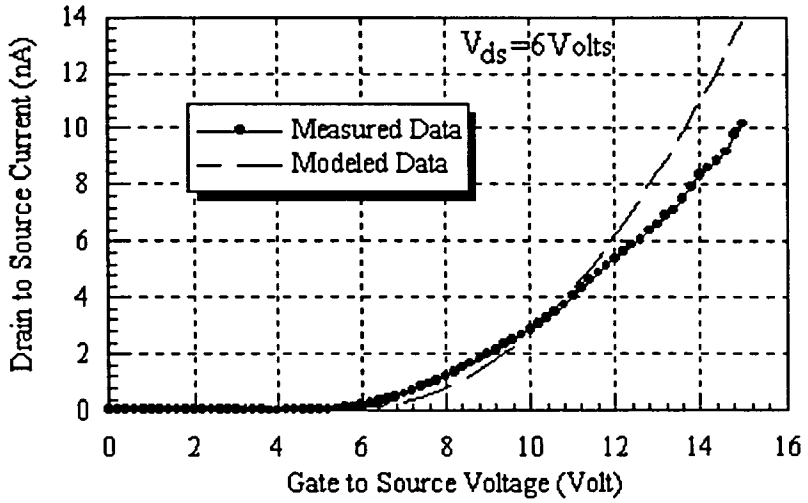

Figure 2.13. Drain to source current versus the gate voltage.

Figure 2.14 plots the measured TFT against the modeled data. The modeled data corresponds well to the measured TFT in the saturation region and in the higher linear region, but in the lower linear region the modeled data does not predict the TFT's behavior well. Again this is due to the i-n+ diode not being incorporated into the model. It should be noted that when the equations were forced to fit the curves the mobility, the density of states, the ON voltage, and the saturation voltage correction factor were varied. Since these parameters are somewhat dependent upon each other, the solution found may not be unique.

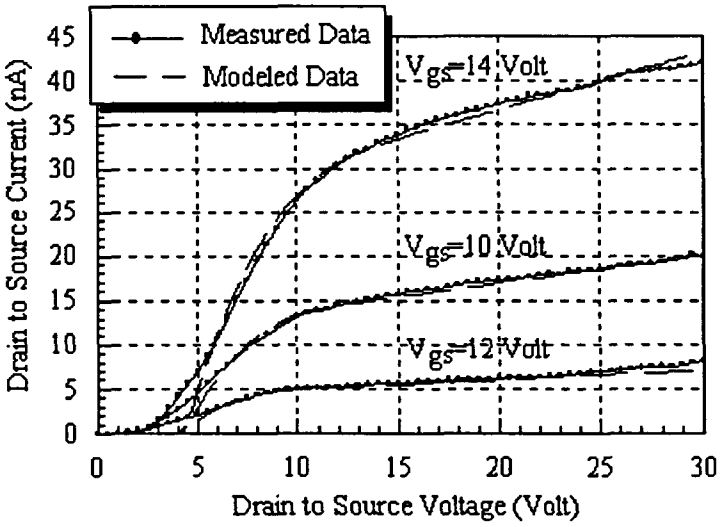

Figure 2.14. Drain to source current versus the drain to source voltage.

3 TFT FABRICATION AND MATERIAL CHARACTERIZATION

A TFT is created on the surface of a non-crystalline substrate. Consequently, the layers must be grown in some kind of a deposition chamber. This means that every layer will depend on specific equipment and may be different than the reported normal. These properties must be studied before the thin-film transistor can be accurately modeled. The material characteristics depend highly upon the type of growth method and the different chemical processes performed upon the device. This chapter will explain how the thin film transistor was fabricated and presents the electrical characteristics of the materials as well as how the characteristics were measured. Only the key process steps will be explained. The complete process traveler is shown in Appendix A.

3.1 Gate Metal

The TFTs will eventually be fabricated on a flexible substrate such as polyimide, but for initial testing purposes the TFT was built on a crystalline silicon wafer with a PECVD silicon dioxide layer of 9000Å. The first layer deposited on the oxide substrate for the inverted TFT topology is the gate metal. The gate metal is evaporated chromium using an electron beam process. The thickness of the metal layer needs to be thin enough so as not to cause step height coverage problems in subsequent layers. The designed thickness of the metal layer is 500Å. The chromium is patterned using conventional step-and-repeat photo lithographical methods: spinning on photoresist, patterning the photoresist, developing the photoresist, etching off the unwanted chromium, and finally removing the photoresist. The device after the metal layer is evaporated and patterned is shown in Figure 3.1.

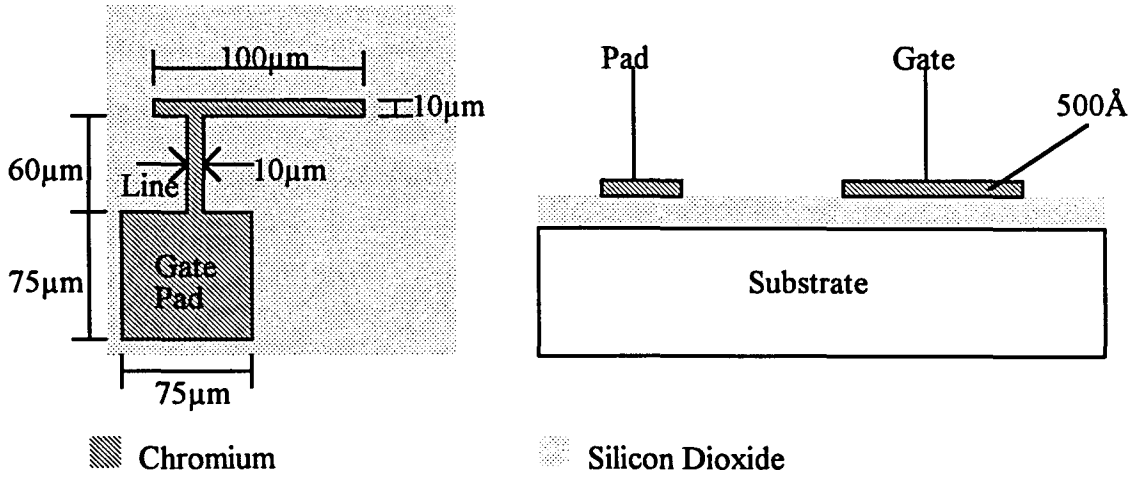

Figure 3.1. Chromium gate layer after processing.

The important characteristic that needs be found from the gate metal is the total electrical resistance. It consists of three different parts; the pad, the line, and the gate. The pads are used to test the gate of the TFT and on average the probe will be set down in the middle of the pad. Therefore, only half of the pad resistance will be used in the calculation. The general formula for calculating resistance is

$$R = R_{Sh} \cdot \frac{L}{W}, \qquad 3.1$$

where R_{sh} is the chromium sheet resistance, L is the metal length, and W is the metal width. The measured value for the sheet resistance of the chromium gate is R_{sh} = 28.8 Ω/□. The calculated resistance of the entire layer is 190.1 Ω.

The advantage of using chromium is that the technology for processing is readily available and it is therefore convenient to use. Furthermore, the next layer, the dielectric layer, seems to grow uniformly upon the surface. Although the metal has a higher resistance, it should not be a problem for most applications, since

little if any current is required by the gate. However, if the resistance of the bottom metal needs to be reduced, an aluminum layer could be deposited first followed by a thin layer of chromium.

3.2 Dielectric Layer

The gate metal must be isolated from the semiconductor by means of an insulator. The insulator will, for the most part, act as a capacitor, attracting charges in the semiconductor on top of the dielectric. The more charges accumulated, the higher the current will be through the semiconductor channel. The general formula for calculating the capacitance is

$$C = \frac{\varepsilon_r \varepsilon_o A}{t}, \qquad 3.2$$

where ε_r is the relative dielectric constant, ε_0 the permittivity of free space, A the area, and t the thickness. The three parameters that will cause the capacitance to be maximized are the area of the device, thickness of the dielectric layer, and the dielectric constant. The area is determined by device geometry or circuit size and the thickness is dependent upon the growth time. As can be seen from Equation 3.2, the thickness should be as thin as possible to create a high capacitance. The third parameter, the dielectric constant, is determined solely by the individual material properties. It is advantageous to select a material with a high dielectric constant, two such candidates are silicon nitride (Si_3N_4) and c-axis vertical oriented aluminum nitride (AlN) which have dielectric constants of ~6 and ~10.5 respectively. Silicon dioxide was not considered due to the high density of interface states between the silicon dioxide and the a-Si:H. Another property the

gate insulator must exhibit is high resistivity in order to allow minimal conduction between the gate and the semiconductor. The insulator deposited on the chrome is shown in Figure 3.2. Silicon nitride is deposited by means of plasma enhanced chemical vapor deposition, while aluminum nitride is deposited by a reactive sputtering process.

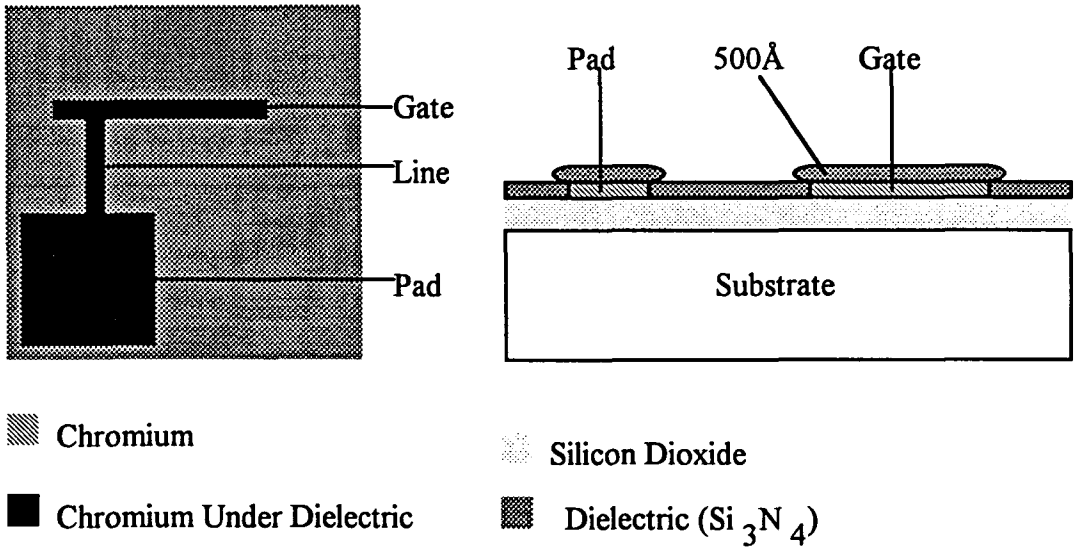

Figure 3.2. TFT device after the dielectric or insulator is deposited.

The capacitance and resistivity properties of the insulator can be determined by fabricating simple capacitors and measuring the capacitance and resistance. Figure 3.3 shows the structure that was used to measure the capacitance and resistance of silicon nitride and aluminum nitride. It should be noted that the measurements were performed using a 1 MHz testing signal.

After the measurements were performed, the thicknesses of the two different dielectrics were found by using an optical system with an index of refraction of 2.14 for aluminum nitride and 2.00 for silicon nitride.

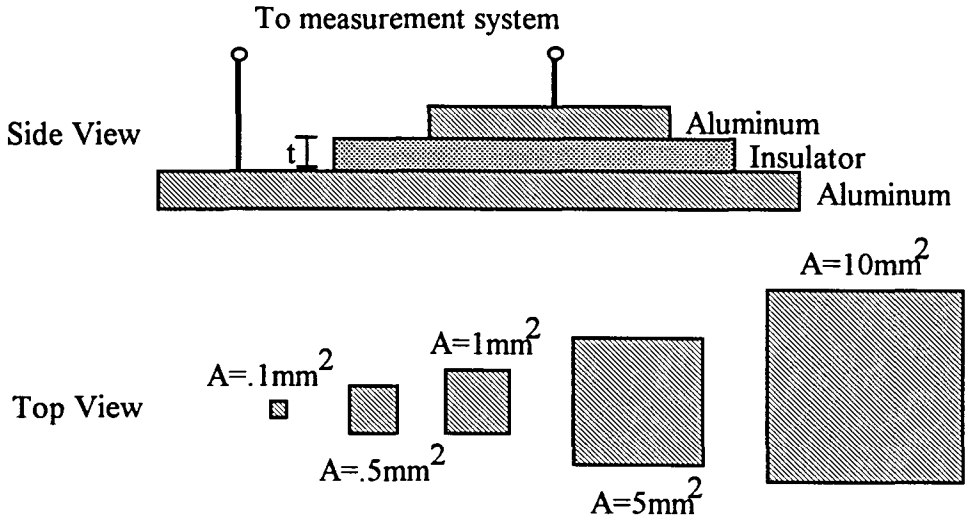

Figure 3.3. Capacitance measurement structure to determine the dielectric constant and resistivity.

For the silicon nitride samples, the thickness measurements were made on the section of the wafer where the bottom metal was removed so as to be consistent with the optical-measurement program. Once the capacitance, resistance, and thickness were obtained, the dielectric constant, ε_r, and the resistivity, ρ, were found by using Equations 3.3 and 3.4.

$$\varepsilon_r = \frac{C \times t}{A \times \varepsilon_0} \qquad 3.3$$

$$\rho = \frac{R \times A}{t} \qquad 3.4$$

Where C is the measured capacitance, t is the dielectric thickness, A is the area of the capacitor, ε_0 is the permittivity of free space, and R is the measured resistance.

Table 3.1 shows the dielectric constants for the silicon nitride samples. The table shows that the dielectric constant is less than the predicted value of 6.0 [12] which implies the material may include oxygen, hydrogen, or both. Table 3.2 shows the calculations for the dielectric constant for aluminum nitride. The dielectric number found is typical for c-axis oriented aluminum nitride as reported by [11].

Table 3.1. Dielectric constant measurements for silicon nitride samples.

Sample #	Mean	Median	Std. Dev.	Thickness (Å)
Cap-2	5.98	5.96	.20	36700
Cap-5	5.51	5.40	.36	4600
Cap-6	5.38	5.34	.23	15300
Cap-7	5.04	5.00	.32	480
Cap-8	5.29	5.30	.12	1460
Average	**5.44**	**5.40**	**.25**	----

Table 3.2. Dielectric constant measurements for aluminum nitride samples.

Sample #	Mean	Median	Std. Dev.	Thickness (Å)
11	11.33	11.31	0.40	7500
14	10.84	10.79	0.36	6500
15	11.09	12.71	3.57	800
16	10.92	10.90	0.54	6500
17	10.28	10.23	0.38	23000
Average	**10.89**	**11.19**	**1.05**	----

Table 3.3 show the calculations for the resistivity of the silicon nitride samples. The numbers are seven orders of magnitude lower than those reported by [12]. This parameter will have to be improved in subsequent device fabrication to permit non-volatile memory storage. This also implies that oxygen and/or hydrogen has been significantly incorporated into the film. Table 3.4 shows the resistivity of the aluminum nitride samples. The resistivity is two to three orders of magnitude lower then those given by [11].

Table 3.3. Resistivity (Ω-cm) measurements for the silicon nitride samples.

Sample #	Mean(Ω-cm)	Median(Ω-cm)	Std. Dev.(Ω-cm)	Thickness (Å)
Cap-2	4.09×10^7	2.98×10^7	4.84×10^7	36700
Cap-5	5.09×10^7	3.41×10^7	1.37×10^8	4600
Cap-6	4.26×10^7	3.49×10^7	4.33×10^7	15300
Cap-7	1.45×10^7	1.10×10^7	1.03×10^7	480
Cap-8	2.32×10^7	1.68×10^7	1.78×10^7	1460
Average	$\mathbf{3.44 \times 10^7}$	$\mathbf{2.53 \times 10^7}$	$\mathbf{5.14 \times 10^7}$	----

Table 3.4. Resistivity (Ω-cm) measurements for aluminum nitride samples.

Sample #	Mean(Ω-cm)	Median(Ω-cm)	Std. Dev.(Ω-cm)	Thickness (Å)
11	4.72×10^6	4.47×10^6	3.73×10^6	7500
14	4.74×10^6	4.02×10^6	3.91×10^6	6500
15	7.94×10^5	4.49×10^5	8.19×10^5	800
16	9.97×10^6	1.01×10^7	7.60×10^6	6500
17	1.36×10^7	1.46×10^7	6.82×10^6	23000
Average	$\mathbf{6.76 \times 10^6}$	$\mathbf{6.73 \times 10^6}$	$\mathbf{4.58 \times 10^6}$	----

3.3 Amorphous Silicon

The amorphous silicon layer is divided into two subparts; compensated intrinsic or p- and heavily doped n+. The layers are grown in a glow discharge system by the decomposition of silane in a hydrogen atmosphere. The compensated intrinsic or p- is grown by adding small amounts of diluted diborane and the n+ is grown by including larger amounts of phosphine. Detailed measurements of the layer were found by growing a sample on a glass substrate and measuring the thickness optically. The growth rate as a function of the silane to hydrogen ratio is shown in Figure 3.4. The data includes samples of the p-, n+, compensated intrinsic, a two layer combination of compensated intrinsic and n+, and p- with a different diborane source.

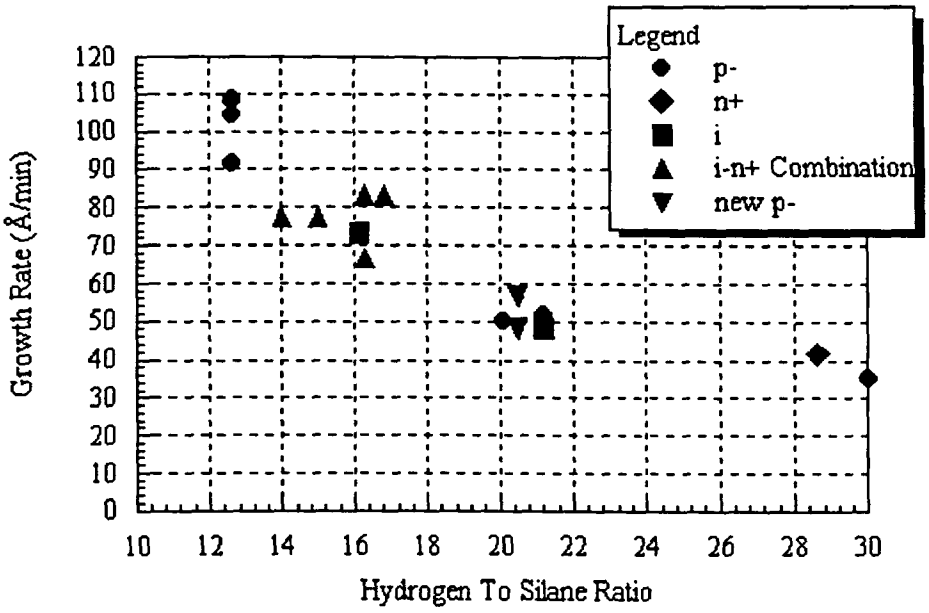

Figure 3.4. Growth rate as a function of hydrogen to silane ratio.

The bandgap of the different types of hydrogenated amorphous silicon is shown in Figure 3.5. The bandgap was found optically by passing different wavelengths of light through the sample and measuring the absorption. The sample was grown on a glass slide and measured in a spectrometer. Typically, a-Si:H has a bandgap of 1.72 eV.

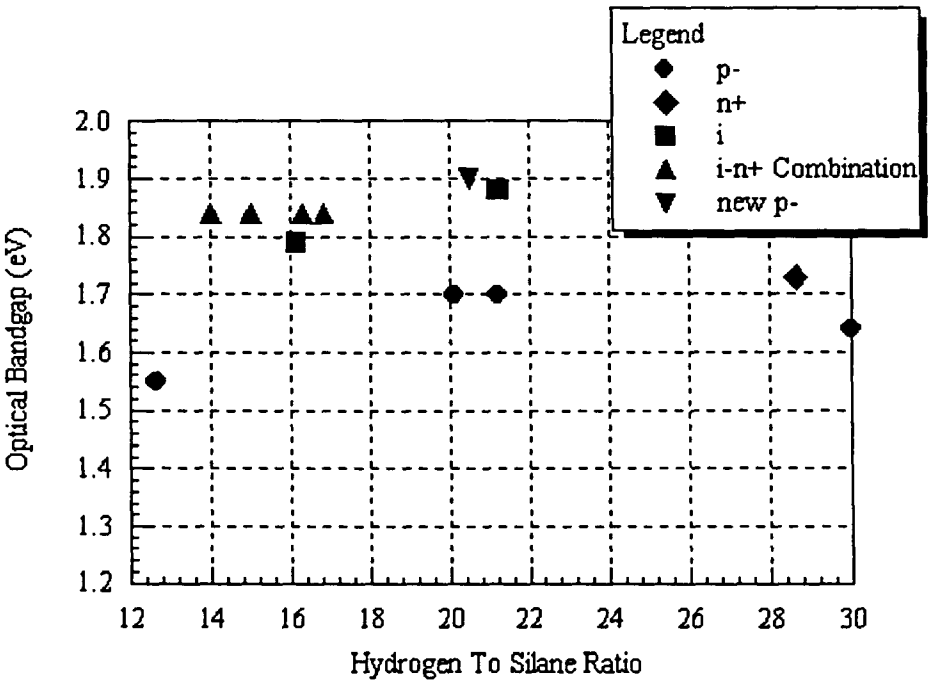

Figure 3.5. Bandgap as a function of hydrogen to silane ratio.

The Fermi level is defined to be the energy where the states have a probability of 1/2 of being occupied. This quantity can be measured by finding the activation energy or the energy between the Fermi-level and the majority carriers band edge. This is measured by heating a sample on a glass slide in a dark environment, passing a current through it, and measuring the resultant conductivity. The activation energy is the slope of the conductivity and

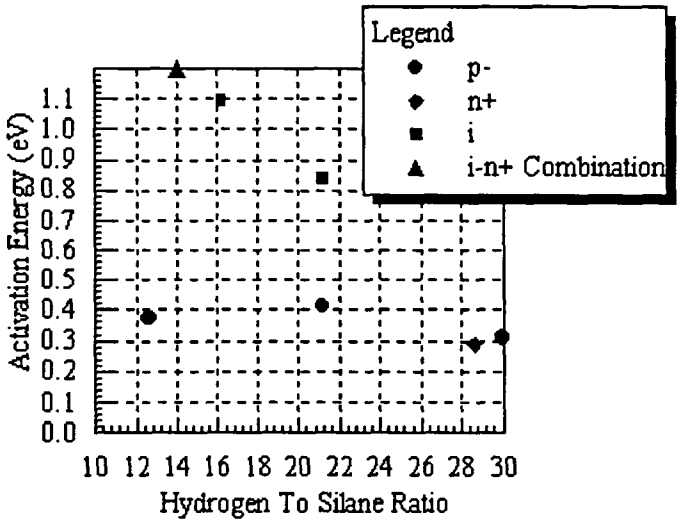

Figure 3.6. Activation energy as a function of hydrogen to silane ratio.

1/Temperature. The measured activation energy is plotted as a function of hydrogen to silane ratio in Figure 3.6.

When the compensated intrinsic and n+ layers are brought into contact, a depletion region is formed and it exhibits a diode like behavior. In order for current to move though the channel, the diode must be first broken down. The current voltage curve is shown in Figure 3.7 and the breakdown voltage is seen to be about -6 Volts.

3.3.1 Compensated Layer

The active layer or the material in which the conductive channel is formed is the compensated intrinsic layer. It is grown in a glow-discharge chamber in a continuous process prior to the n+ layer. When amorphous silicon is grown, there are many more donor-like states in the bottom of the conduction band than the acceptor-like states in the conduction band. This causes the semiconductor to be n-type without any added dopants. Therefore the material needs to be

compensated by adding boron in order to move the Fermi level to a mid-gap energy. The TFT with the amorphous silicon deposited on it is shown in Figure 3.8. As the figure shows, the nominal thickness of the intrinsic region is 500Å. A thickness of 3000Å for the intrinsic region and 500Å for the n+ region

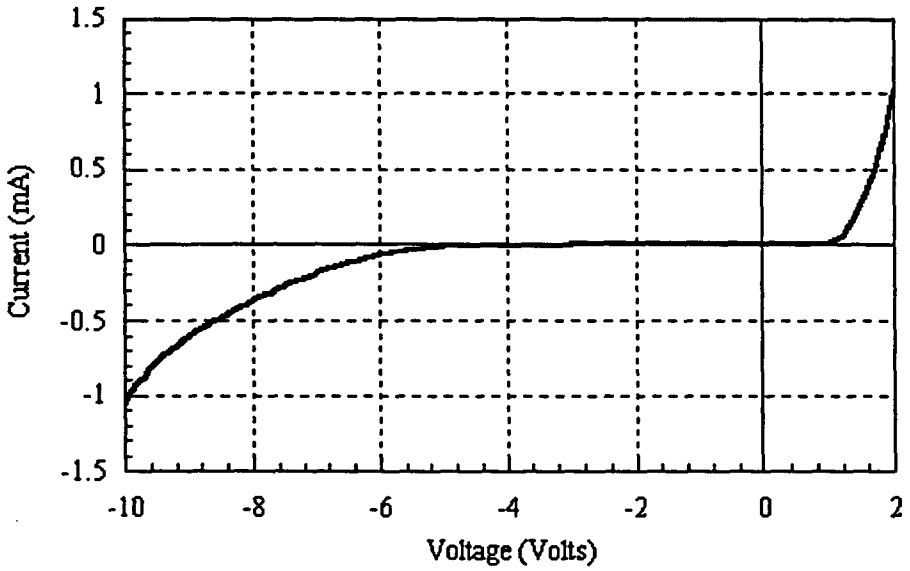

Figure 3.7. I-V characteristics for i-n+ diode.

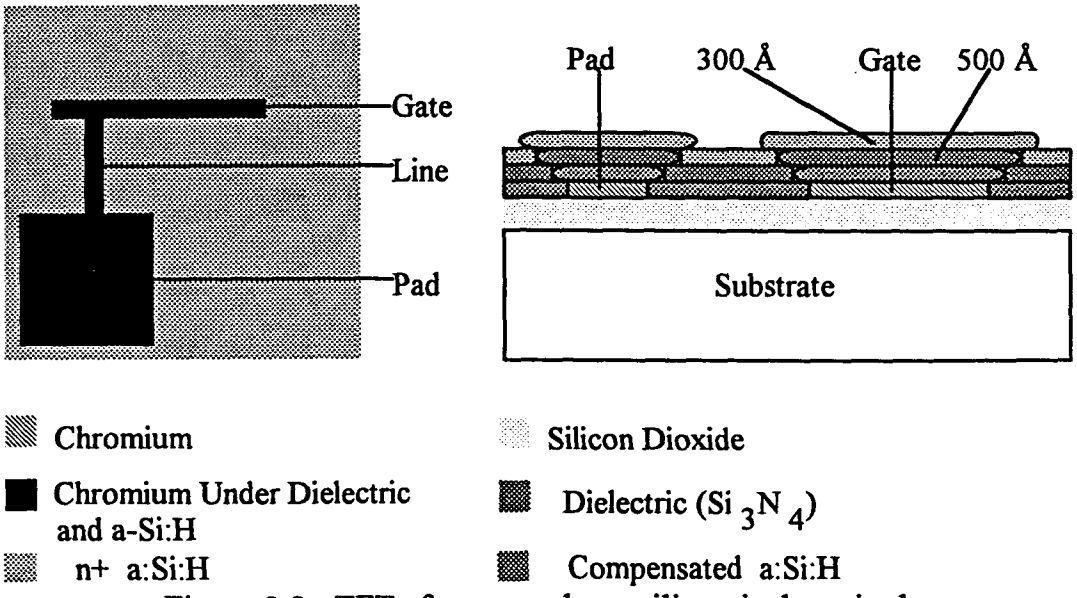

Figure 3.8. TFT after amorphous silicon is deposited.

is also being explored based on [16], but no preliminary information was available at the time of writing.

3.3.2 n+ Layer

The n+ is patterned by spinning photoresist on the wafer, patterning it, and removing the photoresist where the amorphous silicon is to be removed. The exposed n+ layer is removed by reactive ion etching. After the n+ layer is removed, the dielectric and the intrinsic amorphous silicon are removed from the gate vias. The surface is passivated with a layer of silicon dioxide that is grown in a PECVD system. Finally, the silicon dioxide is removed from the gate and n+ regions. The resultant structure is shown in Figure 3.9. As can be seen from the figure, the nominal thickness of the n+ layer is 300Å.

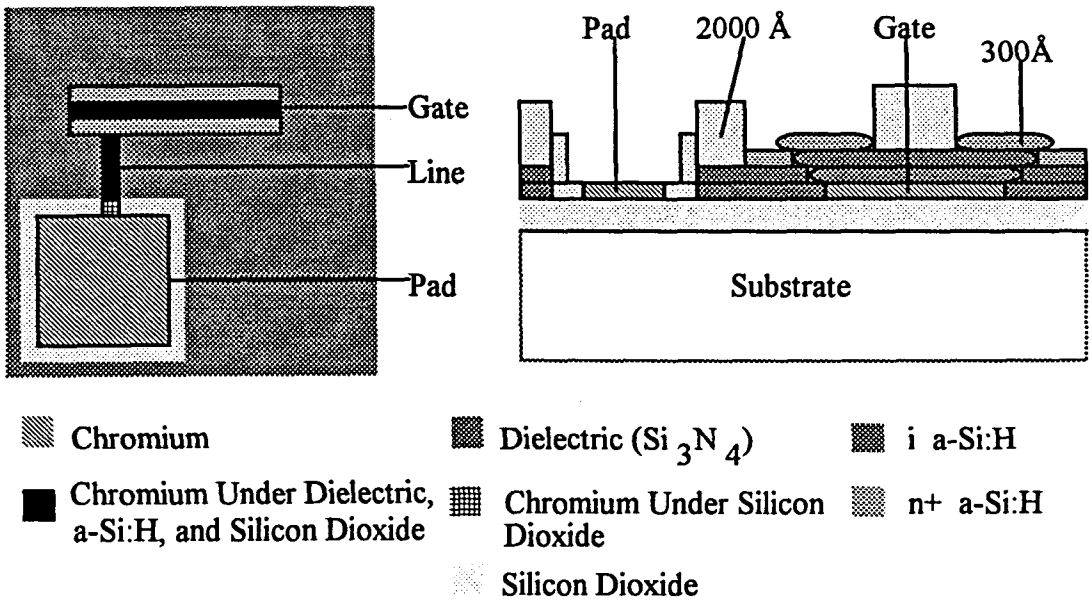

Figure 3.9. TFT after the n+ layer is patterned and silicon dioxide is deposited and patterned.

3.4 Source and Drain Metal

The last layer put on the TFT is the upper gate metal, source contact, and drain contact. They are made out of aluminum evaporated in an electron beam chamber. The thickness of the metal layer needs to be thick to handle the current through the source and drain, the intended thickness is 2,000Å. The aluminum is patterned by a liftoff method: spinning on photoresist, patterning the photoresist, developing the photoresist, depositing aluminum, and finally removing the photoresist along with the overlaying metal. The resultant metal layer is shown in Figure 3.10.

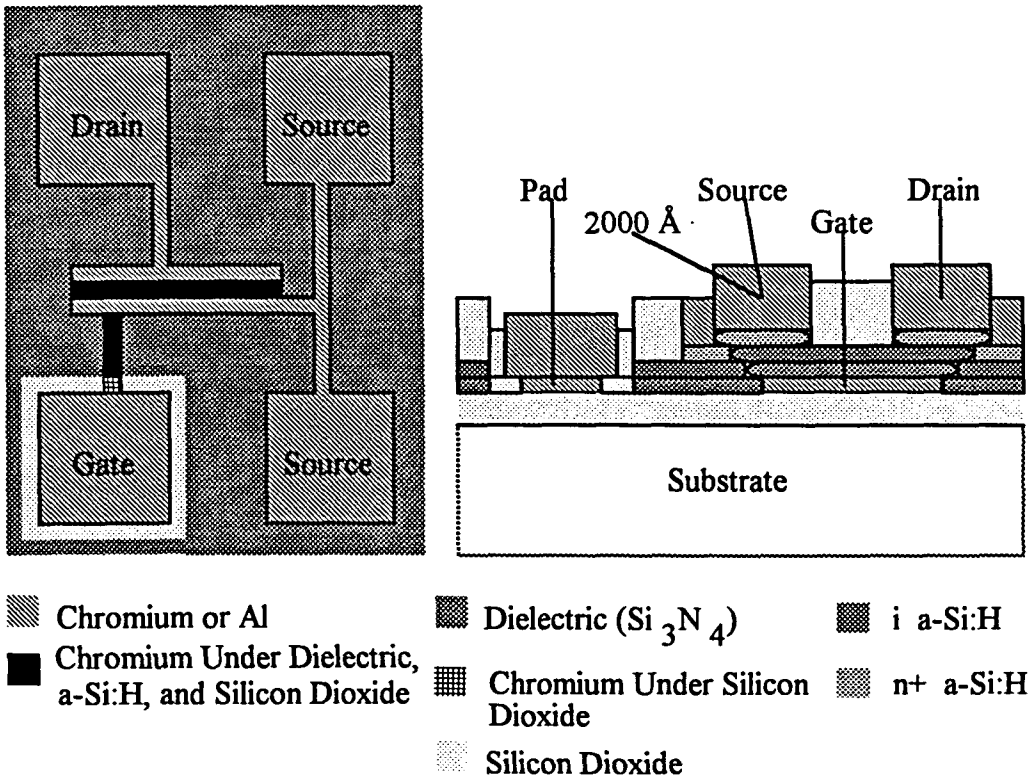

Figure 3.10. TFT after final metal layer.

The only characteristic that needs to be found from the aluminum is the electrical resistance of the pad, contact lines, and the source and drain contacts. The calculated resistance consists of three parts, the pad, the metal line, and the source and drain contacts. The pads are used to probe the source and drain of the TFT and on average the probe will be set down in the middle of the pad. Therefore, only half of the resistance will be taken into account in the calculations. The measured value for aluminum's sheet resistance is $R_{Sh} = 0.23\ \Omega/\square$. Using Equation 3.5 and the measured sheet resistance, the resistance for the source is 4.23Ω and 1.52Ω for the drain.

$$R = R_{Sh} \cdot \frac{L}{W} \qquad 3.5$$

The advantage of using aluminum is that it makes an excellent ohmic contact to the n+ amorphous silicon.

3.5 Conclusion

The first TFTs built did not work even marginally; the I-V characteristics were of an ohmic contact with some gate control. The initial problem was thought to be solved by removing the amorphous silicon from around the gate vias, however, the problem persisted. The problem was later found to be a bad cylinder of diborane, thus making the compensated layer unusable. Once this problem was corrected the devices worked as expected. A typical I-V curve is shown in Figure 3.11 and a picture of the TFT is shown in Figure 3.12.

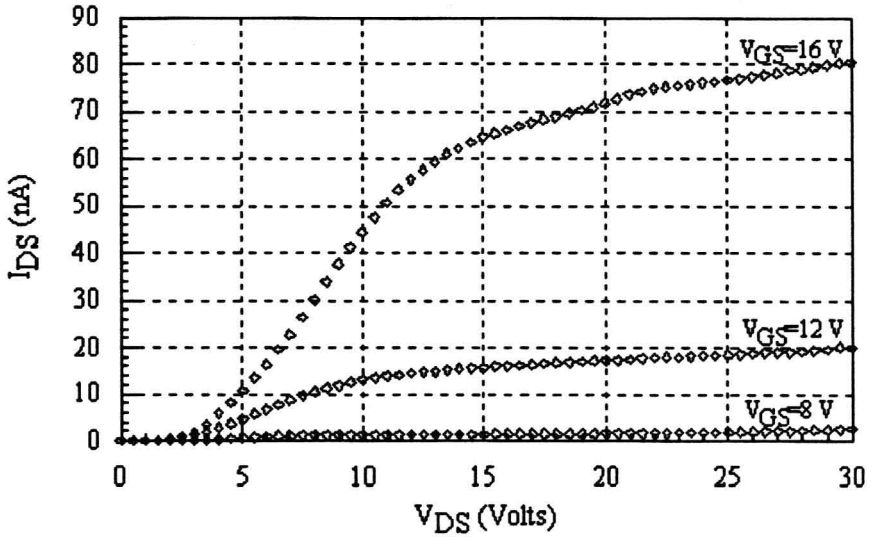

Figure 3.11. I-V curve for a TFT with 100μm gate width.

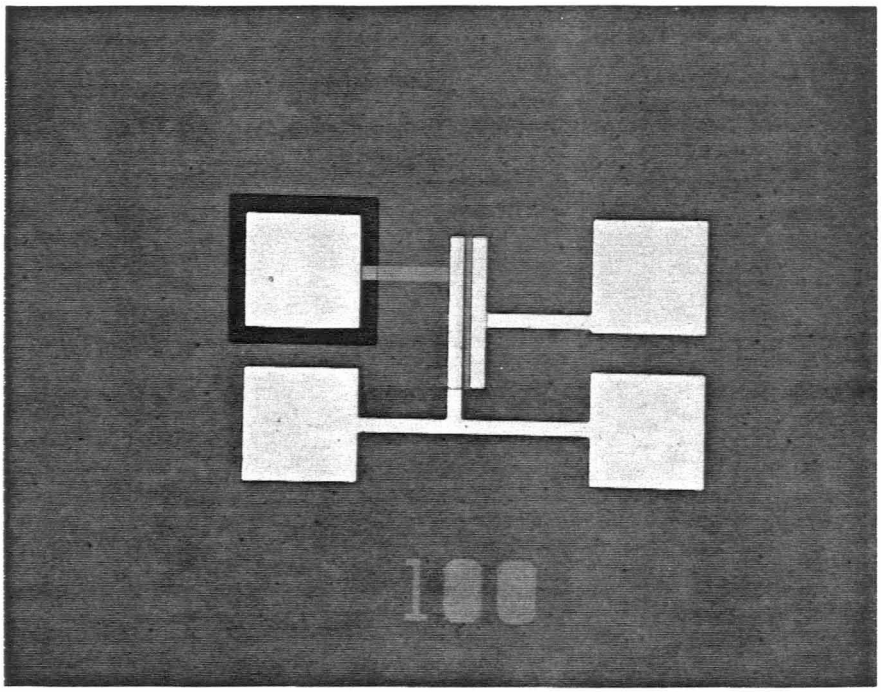

Figure 3.12. Picture of TFT with 100μm gate width.

4 FINDINGS AND RECOMMENDATIONS

4.1 Findings

There are two major findings in this study; the material properties in the fabrication of the TFT and the modeling equation used in simulating the performance of the TFT. The TFT fabrication consists of five different deposition steps: chrome for the gate metal, silicon nitride for the gate dielectric, compensated intrinsic and n+ hydrogenated amorphous silicon, a silicon dioxide passivation layer, and aluminum for the source and drain contacts. Each of these materials were tested and the important material characteristics were found. The chrome metal was found to have a sheet resistance of 28.8 Ω/□ for a thickness of 500Å. This resistivity is about three times higher than the reported bulk value. The dielectric used in the fabrication is silicon nitride with a dielectric constant of 5.4 and a resistivity of 2.53×10^7 Ω-cm. The dielectric constant is much lower than the reported value of 7.5 and the resistivity is much lower than the reported value of 10^{14} Ω-cm. The low values imply that the silicon nitride is a combination of silicon, oxygen, hydrogen, and nitrogen. The amorphous silicon was studied to have an average bandgap of 1.8eV and a growth rate of 58Å/min. for the compensated intrinsic and 42Å/min. for n+. Furthermore, the activation energy for the compensated intrinsic was found to be 0.8eV for intrinsic and 1.1eV for n+. The sheet resistance of the evaporated aluminum deposited on the source and drain was measured at 0.23 Ω/□ at a thickness of 2000Å. The resistivity is about two times higher than the bulk value. The cross sectional view of the TFT after all processing is shown in Figure 4.1.

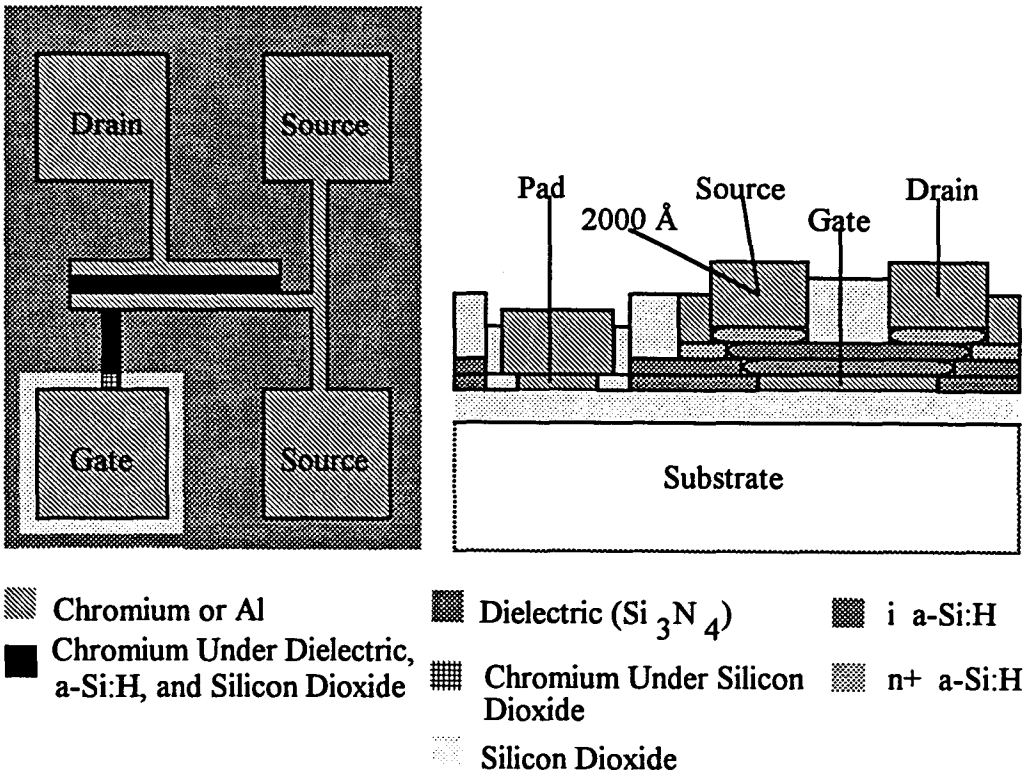

Figure 4.1. TFT after all processing steps.

The second major finding of the research is the modeling equations. The modeling equations presented were the traditional MOSFET level 1 and the fundamental device equations. Figure 4.2 shows the measured data against the predicted MOSFET data for I_{ds} versus V_{ds}. The MOSFET model was found not to predict the behavior of the TFT well, due to the fact that the model assumes all of the induced charge is present in the conduction band. The new model's I_{ds} versus V_{ds} plot is shown in Figure 4.3. The model predicts the behavior well in the saturation region and in the upper linear region. However, in the lower region, the model fails to predict the behavior due to the fact the model does not incorporate the i-n+ source and drain diodes.

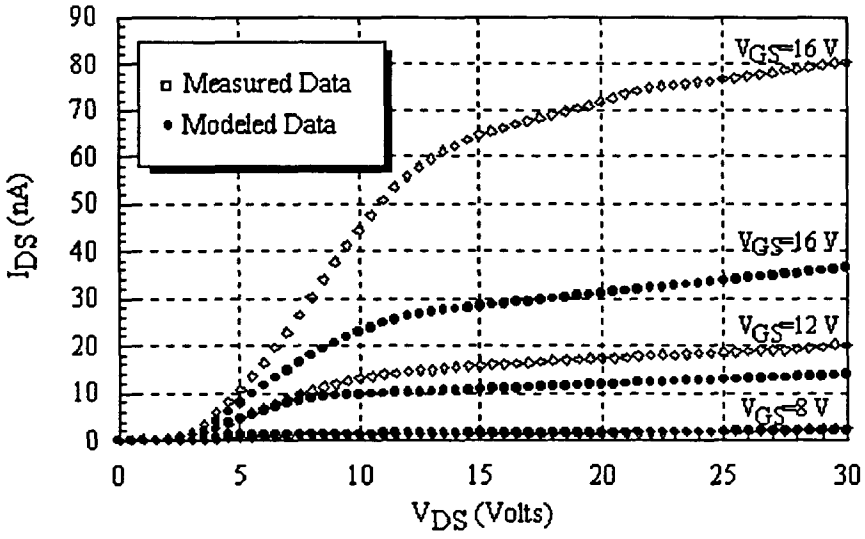

Figure 4.2. Results of model based on the MOSFET level 1 equations.

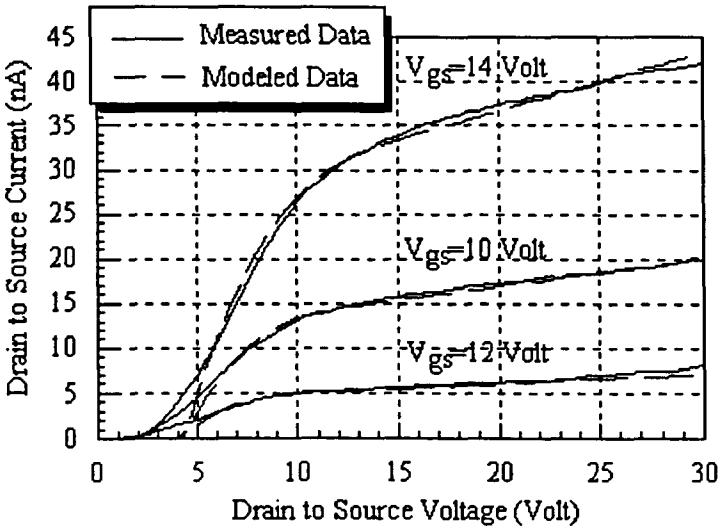

Figure 4.3. Results of model based on fundamental device equations.

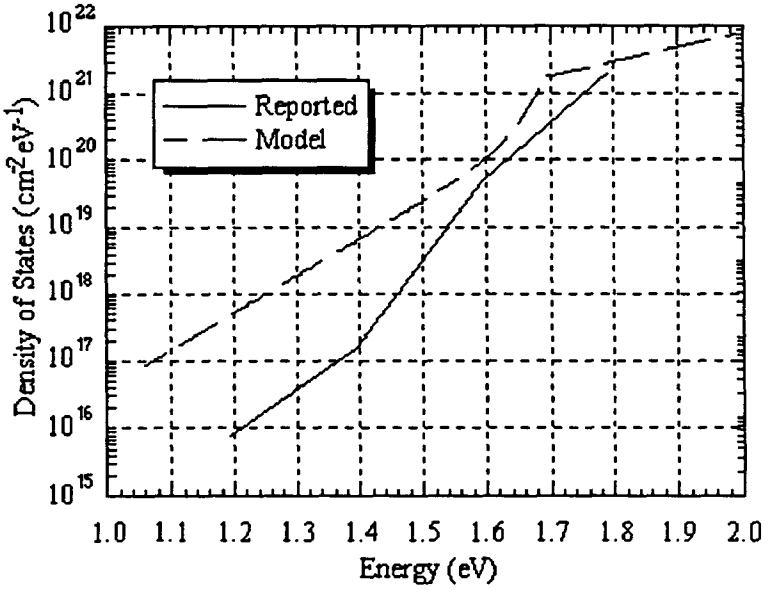

Figure 4.4. Density of states from the model based on fundamental device equations and those reported by [8].

Figure 4.4 compares the density of states from the model based on fundamental device equations to the density of states as reported from [8]. The conduction band and the tail states close to the conduction band seem to be in good agreement. However, the deep states are significantly different and it is for this reason the project's TFTs have a low saturation current for reasonable gate to source voltages. The a-Si:H needs significant improvement for higher performance TFTs.

4.2 Recommendations

One of the major sources of error in the modeling equations is predicting the behavior in the sub-linear region. The I-V modeling equations need to include the effect of the i-n+ diodes at the source and at the drain. This addition will model the lower linear region with a greater degree of accuracy while not effecting

the upper linear and saturation regions. Another source of error may be due to the fact that the density of states and mobility were found from the modeling equations. The density of states or the band mobility for the amorphous silicon needs to be found independently of the equations. This process includes creating an n-i-n diode and measuring the absorption spectrum. An interesting test for the model would be to apply it to typical a-Si:H found in the literature. The model also needs further refinement to include the capacitance properties. This should be fairly simple to accomplish since several papers included in the bibliography outline the procedure.

Current work on the project is directed toward adding a floating gate to the TFT. The integrated circuit has been designed, but the fabrication has not been completed at the time of this writing. Initial designs for the roll-to-roll processing system is also being contemplated. Future work on the project will consist of perfecting the roll-to-roll process and integrating the TFT and the floating gate TFT into the roll-to-roll process. The biggest challenge will be in patterning the photo-resist.

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Special appreciation is reserved for Russ Bruhn whose friendship has helped me take life a little less seriously; for Kamal Avala, Eric Michel, Joel Fastenau, Ed Goff, and Scott Deboer whose encouragement and friendship have kept me inspired.

APPENDIX A: PROCESS TRAVELER FOR THE TFT

Process:	DARPA TFT	**Lot No: D-011493**	
Revision:	May 1, 1993	**Wafer No: 7,11,12,13**	

Note: #7,12 Xerox process, #11,13 MRC's

No.	Step	Process	Side	Parameters
1	Deposit Oxide	PECVD oxide	f	System: PECVD Chemistry:N2O(35 sccm)+SiH4(20 sccm)@400mT Temperature: 220C Power: 13W Thickness: 9000 Comments:
2	Pattern Alignment Marks	Pattern PR	f	Mask #0: Standard alignment marks
		Wet Oxide Etch	f	Chemistry: BHF
		Strip PR	f	Chemistry: Acetone, methanol, DI
3	Deposit Gate Metal	Evaporate Cr	f	System: Thermal evaporation Chemistry: Chromium Thickness: 500A
4	Pattern Gate Metal	Pattern PR	f	Mask #1: Gate metal
		Wet Etch Cr	f	Chemistry: CR4 photomask etch
		Strip PR	f	Chemistry: Acetone, methanol, DI
		O2 Plasma Ash	f	System: RIE Chemistry: O2 plasma
		Strip PR	f	Chemistry: Acetone, methanol, DI
5	Deposit Gate Dielectric	PECVD Nitride	f	System: PECVD Chemistry: SiH4(20sccm)+NH3(55sccm)@400mT Temperature: 220C Power: 13W Thickness: #11 & 13: 750 A, #7 & 12: 3000A Comments:

6	Deposit Amorphous Silicon	PECVD a-Si(i)	f	System: PECVD system 5 Chemistry:SiH4:H2(200sccm)+H2(100sccm)@300mT Temperature: 275C Power: 12.5W Thickness: #11 & 13: 1500A, #7 & 12: 750A Comments:
		PECVD a-Si(n+)	f	System: PECVD system 5 Chemistry:SiH4:H2(200sccm)+H2(100sccm) +PH3(5(sccm)@350mT Temperature: 275C Power: 12.5W Thickness: #11 & 13: 750A, #7 & 12: 500A Comments:
7	Pattern n+ Contacts	Pattern PR	f	Mask #2: N+ protect
		Dry Etch a-Si	f	System: RIE Chemistry: O2 + CHF3 Etching Potential: 435 Volts DC Etch Stop: Timed etch, stop on a-Si (i)
		Strip PR	f	Chemistry: Acetone, methanol, DI
8	Pattern Via Surround	Pattern PR	f	Mask #3: Via surround
		Dry Etch a-Si	f	System: RIE Chemistry: O2 + CHF3 Etching Potential: 435 Volts DC Etch Stop: Stop on chromium
		Strip PR	f	Chemistry: Acetone, methanol, DI
9	Deposit Oxide Passivation	PECVD Oxide	f	System: PECVD Chemistry:N2O(35sccm)+SiH4(20sccm)@400mT Temperature: 220C Power: 13W Thickness: 1500 A Comments:

10	Pattern Via	Pattern PR	f	Mask #4: Vias & n+ windows
		Dry Etch Oxide	f	System: RIE Chemistry:CHF3(45sccm)+O2(5sccm)@40mT Etching Potential: 435 Volts DC Etch Stop: Stop on chromium
		Strip PR	f	Chemistry: Acetone, methanol, DI
11	Pattern Metal Interconnect	Pattern	f	Mask #5: Top metal
12	Deposit Metal Interconnect	Evaporate Al	f	System: E-beam Chemistry: Aluminum Thickness: 2000A Comments:
13	Metal Lift-off	Strip PR	f	Chemistry: NMP, methanol, DI
99	Finish			Comments:

APPENDIX B: MATHCAD™ IMPLEMENTATION OF MOSFET LEVEL 1 EQUATIONS

This Mathcad file models a MOSFET using the standard modeling equations. The file is broken up into two sections. The first section contains unit definitions and constant definitions while the second section shows the device equations as well as sample output graphs.

Section #1

Since Mathcad does not contain certain units, they must first be defined.

$um \equiv 1 \cdot 10^{-6} \cdot m$	Micron
$ev \equiv 1.602189 \cdot 10^{-19} \cdot joule$	Electon Volt
$Ang \equiv 1 \cdot 10^{-10} \cdot m$	Angstrom

The changeable constants that define the TFT characteristics

$V_{ON} := 3.0 \cdot volt$	On Voltage
$\mu := .00021 \cdot \frac{cm^2}{volt \cdot sec}$	Conduction band mobility
$\varepsilon_{SiN} := 5.4$	Dielectric constant of the insulator
$t_{ox} := 500 \cdot Ang$	Dielectric thickness
$W := 100 \cdot um$	Width of the gate
$L := 10 \cdot um$	Length of the gate
$X_{jl} := 2.5 \cdot um$	Diffusion/Oxide Overlap
$V_{TH} := 5.6 \cdot volt$	Threshold Voltage
$\lambda := 0.025 \cdot \frac{1}{volt}$	Channel Length Modulation Factor

Constants that can not be changed.

$\varepsilon_o := 8.85418782 \cdot 10^{-12} \cdot \frac{farad}{m}$	Permitivity of free space
$C_{ox} := \frac{\varepsilon_{SiN} \cdot \varepsilon_o}{t_{ox}}$	Oxide capacitance
$KP := \mu \cdot C_{ox}$	Transconductance Parameter

Section #2

Define equations for the crystalline MOSFET

Equation is valid in the linear region (Vgs > Vth and Vds<Vgs-Vth)

$$IDS_{lin}(V_{DS}, V_{GS}) := KP \cdot \frac{W}{L - 2 \cdot X_{jl}} \cdot \left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right) \cdot V_{DS} \cdot (1 + \lambda \cdot V_{DS})$$

Equation is valid in the saturation region (Vgs>Vth and Vds>Vgs-Vth)

$$IDS_{sat}(V_{DS}, V_{GS}) := \frac{KP}{2} \cdot \frac{W}{L - 2 \cdot X_{jl}} \cdot (V_{GS} - V_{TH})^2 \cdot (1 + \lambda \cdot V_{DS})$$

Equation is valid in the sub-threshold region (Vgs<Vth)

$$IDS_{sub}(V_{DS}, V_{GS}) := 0 \cdot amp$$

Determine which region the transistor is operating in

$$I1_{DS}(V_{DS}, V_{GS}) := if(V_{DS} \le V_{GS} - V_{TH}, IDS_{lin}(V_{DS}, V_{GS}), IDS_{sat}(V_{DS}, V_{GS}))$$

$$I2_{DS}(V_{DS}, V_{GS}) := if(V_{GS} < V_{TH}, IDS_{sub}(V_{DS}, V_{GS}), I1_{DS}(V_{DS}, V_{GS}))$$

$$I_{DS}(V_{DS}, V_{GS}) := if(V_{DS} \le V_{ON}, 0 \cdot amp, I2_{DS}(V_{DS} - V_{ON}, V_{GS}))$$

Create a range of voltages for the drain to source voltage to be swept and read in the measured data to compare to the modeled data.

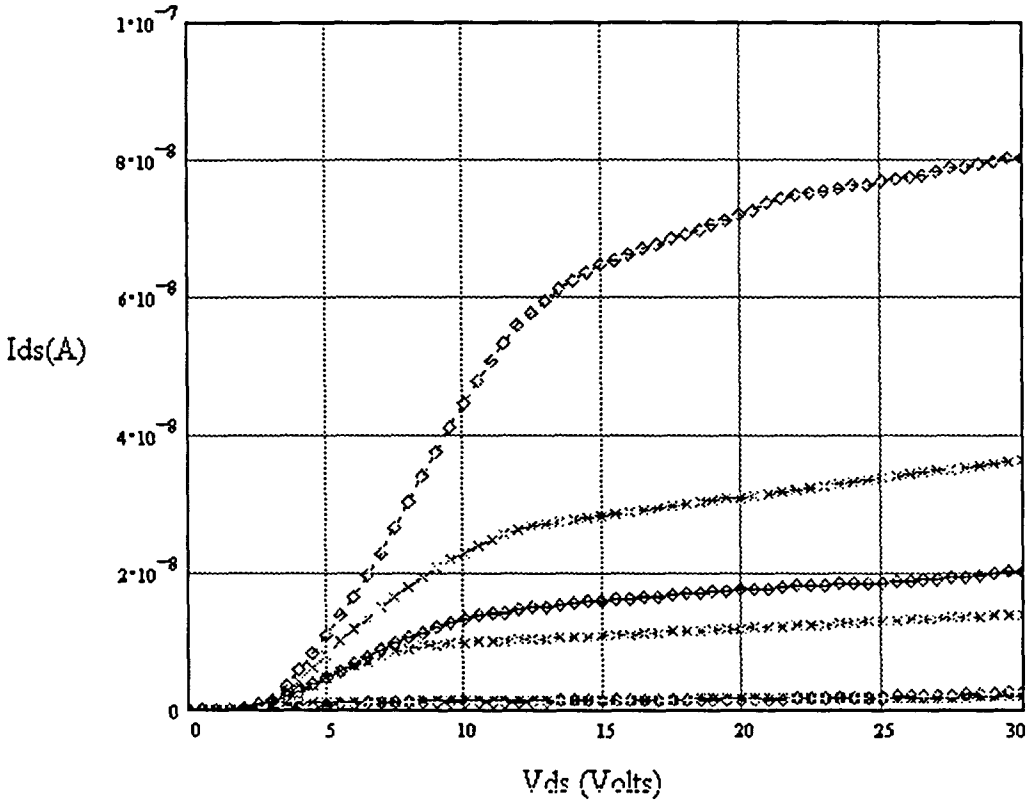
$VGS := READPRN(TFTVGS_{TXT}) \cdot volt$ $\quad IGS := READPRN(TFTI\_VGS_{TXT}) \cdot 10^{-9} \cdot amp$

$VDS := READPRN(TFTVDS_{TXT}) \cdot volt$ $\quad IDS := READPRN(TFTI\_VDS_{TXT}) \cdot 10^{-9} \cdot amp$

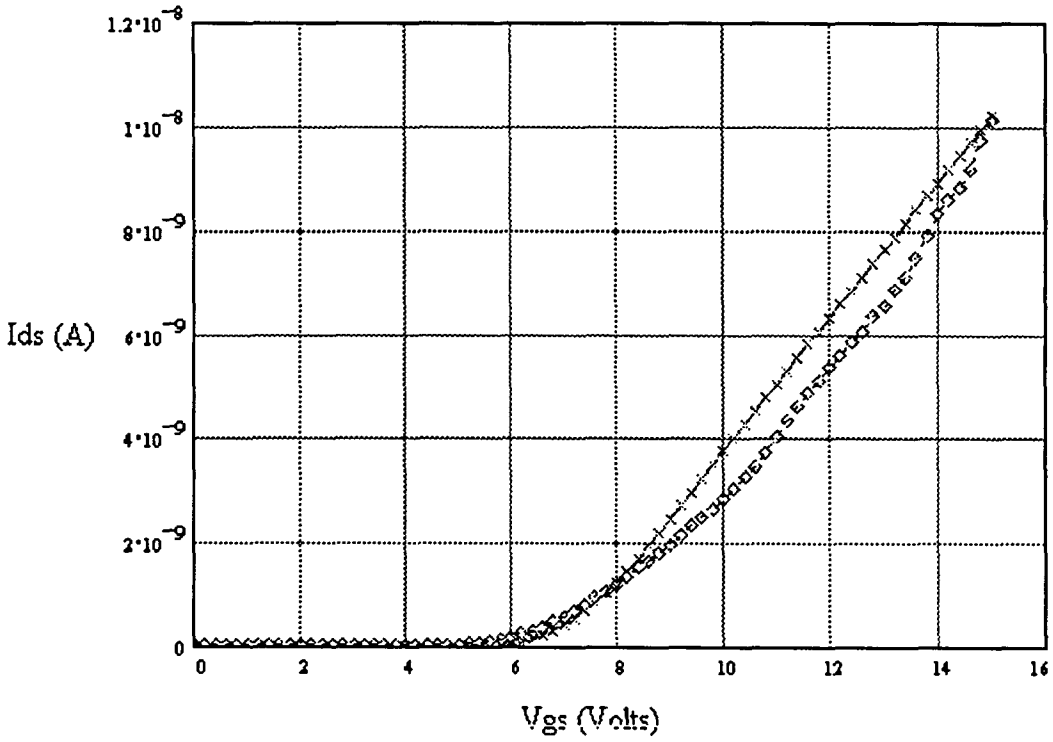
$gs := 0..length(VGS) - 1$

$ds := 0..length(VDS) - 1$

Graph out the results of the calculations



Diamonds : Measured Data
xs : Modeled Data



Diamonds : Measured Data
xs : Modeled Data

APPENDIX C: MATHCAD™ IMPLEMENTATION OF THE FUNDAMENTAL DEVICE EQUATIONS TO MODEL A TFT

This Mathcad file models a TFT using fundumental physics equations. The file is broken up into two sections. The first section contains unit definitions and constant definitions while the second section shows the device equations as well as sample output graphs.

Section #1

Since Mathcad does not contain certain units, they must first be defined.

$um \equiv 1 \cdot 10^{-6} \cdot m$	Micron
$ev \equiv 1.602189 \cdot 10^{-19} \cdot joule$	Electon Volt
$Ang \equiv 1 \cdot 10^{-10} \cdot m$	Angstrom

The changeable constants that define the TFT characteristics

$W := 100 \cdot um$	Width of the gate
$L := 7.5 \cdot um$	Length of the gate
$d := 0.05 \cdot um$	Dielectric thickness
$\mu_{Band} := .0034 \cdot \frac{cm^2}{volt \cdot sec}$	Conduction band mobility
$V_{FB} := 2.0 \cdot volt$	Flat band Voltage
$V_{On} := 4.3 \cdot volt$	On Voltage
$\lambda := .025 \cdot volt^{-1}$	Channel Length Modulation Factor
$T := 300 \cdot K$	Temperature
$E_g := 1.7 \cdot ev$	Energy gap
$Na_{Deep} := 1 \cdot 10^{11} \cdot \frac{cm^{-3}}{ev}$	DOS acceptor-like constant for deep states
$Na_{Tail} := 1 \cdot 10^{-14} \cdot \frac{cm^{-3}}{ev}$	DOS acceptor-like constant for tail states
$Ea_{Deep} := 7.8 \cdot 10^{-2} \cdot ev$	Energy for acceptor-like constant for deep states

$Ea_{Tail} := 2.1 \cdot 10^{-2} \cdot ev$	Energy for acceptor-like constant for deep states
$Ea_{Band} := 2 \cdot 10^{-1} \cdot ev$	Energy for acceptor-like constant for band states
$\varepsilon_i := 5.4$	Dielectric constant of the insulator
$E_i := 1.05785 \cdot ev$	Fermi level in intrinsic amorphous silicon
$\varepsilon_s := 11.0$	Dielectric constant for the amorphous silicon
$Vn := .8$	Saturation Voltage Correction Factor

Constants that can not be changed.

$q := 1.6021917 \cdot 10^{-19} \cdot coul$	Electron's charge
$k := 1.380658 \cdot 10^{-23} \cdot \frac{joule}{K}$	Boltzmann's constant
$E_c := E_g$	Conduction band edge
$E_v := 0 \cdot ev$	Valence band edge
$E_\infty := 9 \cdot ev$	Energy level at infinity
$\varepsilon_0 := 8.854187817 \cdot 10^{-12} \cdot \frac{farad}{m}$	Permitivity of free space
$q1 := \frac{ev}{volt}$	Electron charge/Voltage conversion factor

Section #2

The first task is to define equations to calculate the the space charge density as a function of energy. This requires the trapped charge density and free charge density to be defined. In order to find these, the Fermi-level and the DOS for acceptor like states must be defined.

Define the fermi function

$$f(E, E_f) := \frac{1}{1 + e^{\frac{E - E_f}{k \cdot T}}}$$

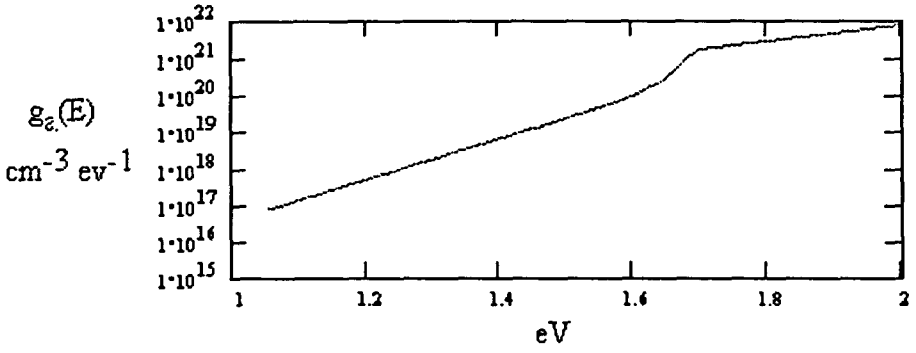
Create a series for energy to graph out the defined functions.

$N := 300$ $\quad bg := 0..N$

$$E_{bg} := \frac{bg}{N} \cdot (2 \cdot ev - E_i) + E_i \qquad E2_{bg} := \frac{bg}{N} \cdot (E_\infty - E_i) + E_i$$

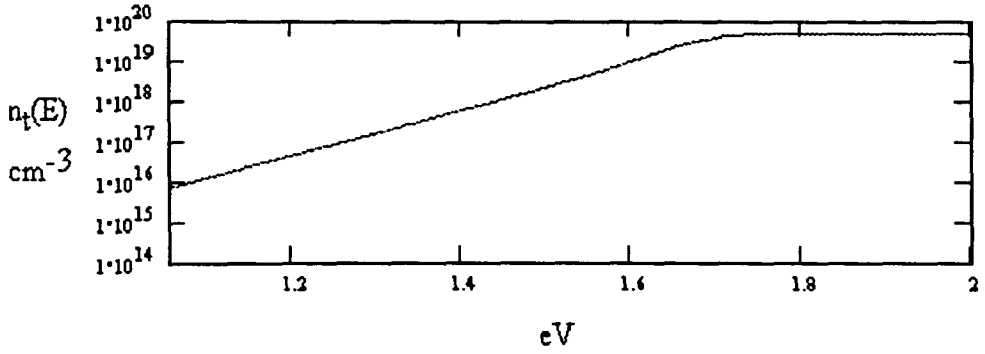
The DOS function is broken up into two parts; bandgap and conduction band. The conduction band states are defined at the point where E>=Ec.

$$g_a(E) := \text{if}\left[E \geq E_c, \left(Na_{Deep} \cdot e^{\frac{E_c}{Ea_{Deep}}} + Na_{Tail} \cdot e^{\frac{E_c}{Ea_{Tail}}}\right) \cdot e^{\frac{E-E_c}{Ea_{Band}}}, Na_{Deep} \cdot e^{\frac{E}{Ea_{Deep}}} + Na_{Tail} \cdot e^{\frac{E}{Ea_{Tail}}}\right]$$



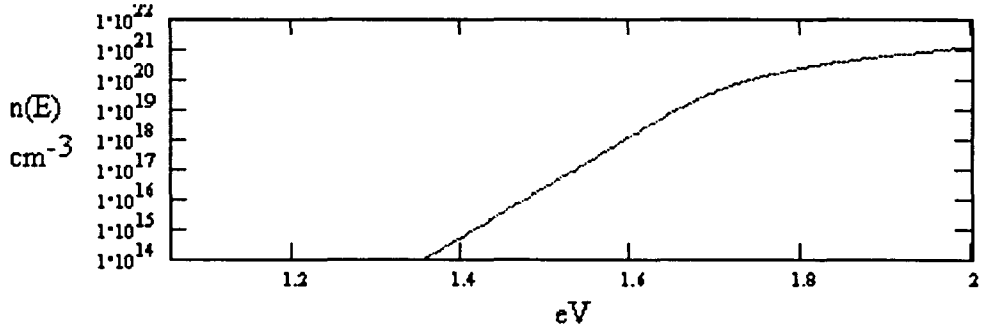
The trapped electrons in the energy gap is found by integrating the DOS function times the Fermi-level over the band gap.

$$n1_t(E_f) := \int_{E_v}^{E_c} g_a(E) \cdot f(E, E_f)\, dE \qquad n2_{t_{bg}} := n1_t(E2_{bg}) \qquad n_t(E) := \text{linterp}(E2, n2_t, E)$$



The free electrons in the conduction band is calculated by integrating Nd times the Fermi-level from the conduction band edge to infinity.

$$n1(E_f) := \int_{E_c}^{E_\infty} g_a(E) \cdot f(E, E_f)\, dE \qquad n2_{bg} := n1(E2_{bg}) \qquad n(E) := \text{linterp}(E2, n2, E)$$



The space-charge density is defined as the number of electrons times the electrons charge.

$$\rho(E_f) := -q\cdot\left(n_t(E_f) + n(E_f)\right)$$

The next task is to calculate the induced charge at the source as a function of gate voltage. Because the calculations are calculation intensive, a range of variables will be calculated first and a linear interpolation will be used to find the other values.

All of the functions in this section are calculated from a series of voltages located at the semiconductor insulator interface. From previous calculations, the range of Vs has been determined to be .7 volts.

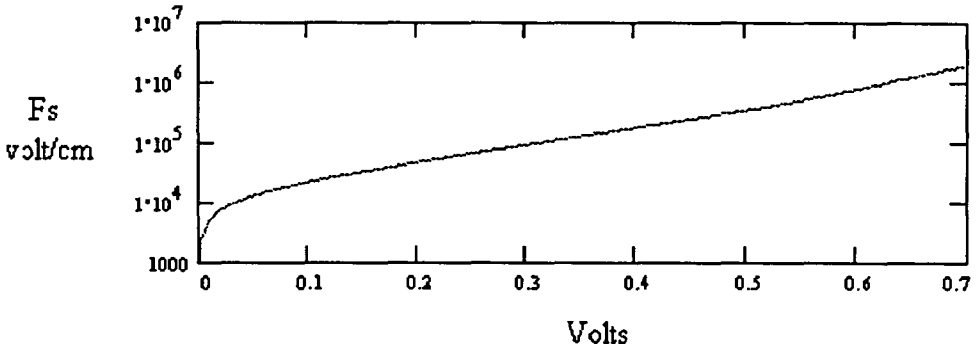
$$ss := 0..N$$

$$V_{ss} := \frac{ss}{N}\cdot .7\cdot volt$$

The electric field at the interface, Fss, is calculated by solving Poisson's equation. The electric field is also found as a function of Vss. The electric field is not allowed to go to zero since it will cause a singularity later.

$$F_{ss} := \sqrt{\frac{2}{\varepsilon_s\cdot\varepsilon_0\cdot q}\cdot\left(\int_{E_i}^{E_i + q1\cdot V_{ss}} -\rho(E)\,dE\right)}$$

$$F_s(V_s) := \text{if}\left(V_s = 0\cdot volt,\ 1\cdot\frac{volt}{m},\ \text{linterp}(V, F, V_s)\right)$$



The induced charge at the source is a simple function of the electric field at the interface. The induced charge is also not allowed to go to zero to avoid division by zero errors.

$$n_{in_{ss}} := \frac{\varepsilon_s \cdot \varepsilon_0 \cdot |F_{ss}|}{q}$$

$$n_{in_0} := 1 \cdot cm^{-2}$$

$$nl_{ind}(V_s) := \frac{\varepsilon_s \cdot \varepsilon_0 \cdot |F_s(V_s)|}{q}$$

The gate voltage is also calculated as a function of the electric field and the interface potential, Vs.

$$V_{g_{ss}} := V_{ss} + \frac{\varepsilon_s \cdot F_{ss} \cdot d}{\varepsilon_i} + V_{FB}$$

With all the available vectors, the induced charge at the source can be found as a function of gate voltage.

$$n_{inds}(V_{gs}) := if\left(V_{gs} \le V_{FB}, 0 \cdot cm^{-2}, nl_{ind}\left(linterp\left(V_g, V, V_{gs}\right)\right)\right)$$

The next step is to find the mobility as a function of the induced charge. This is defined as the ratio of free carriers in the conduction band to the total number of induced charges times the band mobility.

The free carrier density in the conduction can be found as a function of the interface potential by the following formula. It also must not be allowed to go to zero.

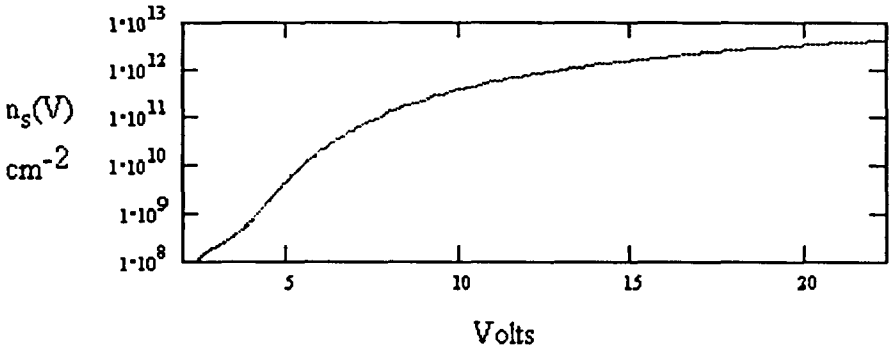
$$n_{s_{ss}} := \frac{1}{q} \cdot \int_{E_i}^{E_i + q1 \cdot V_{ss}} \frac{n(E)}{F_s\left[q1^{-1} \cdot (E - E_i)\right]} dE$$

$N1 := 100$

$t := 0..N1$

$$E1_t := \frac{t}{N} \cdot (q1 \cdot V_{ss}) + E_i$$

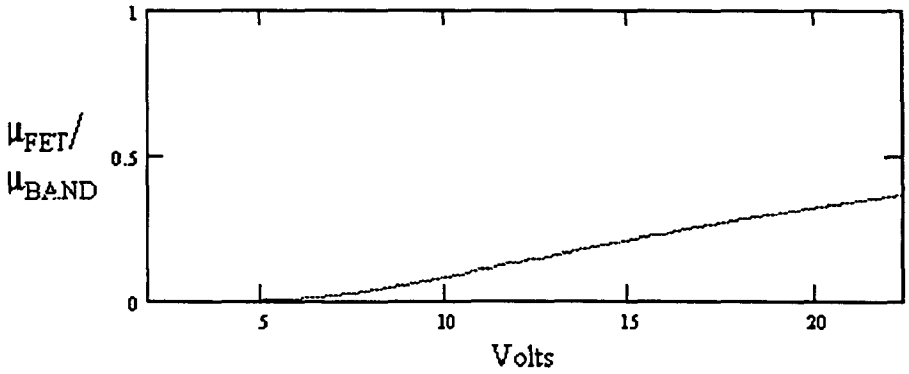
$$n_{s_0} := 1 \cdot 10^{-2} \cdot cm^{-2}$$



The field effect mobility is the ratio of the electrons in the conduction band divided by the total charge. The mobility is also given as a linear regression.

$$\mu_{ss} := \frac{n_{s_{ss}}}{n_{in_{ss}}}$$

$$\mu_{FET}(n_{inds}) := \mu_{Band} \cdot linterp(n_{in}, \mu, n_{inds})$$



The last task is to calculate the current using the constants defined above, the induced charge at the drain, and the field effect mobility. The current must be a function of the drain to source voltage and the gate to source voltage.

The electron concentration induced at the drain is a function of the electron concentration at the source minus the potential between the source and drain using the gradual channel approximation

$$n_{indd}(V_{gs}, V_{ds}) := if\left[\left(n_{inds}(V_{gs}) - \frac{\varepsilon_i \cdot \varepsilon_o \cdot V_{ds} \cdot Vn}{q \cdot d}\right) \le 0 \cdot cm^{-2}, 0 \cdot cm^{-2}, n_{inds}(V_{gs}) - \frac{\varepsilon_i \cdot \varepsilon_o \cdot V_{ds} \cdot Vn}{q \cdot d}\right]$$

The saturation voltage is defined as the voltage that causes the induced charge at the drain to be zero.

$$V_{ds} := 5 \cdot volt$$

$$V_{dsat}(V_{gs}) := root\left(n_{inds}(V_{gs}) - \frac{\varepsilon_i \cdot \varepsilon_o \cdot V_{ds}}{q \cdot d}, V_{ds}\right)$$

The current through the induced channel is defined as follows.

$$I_O(V_{gs}, V_{ds}) := q^2 \cdot \left(\frac{W}{L}\right) \cdot \left(\frac{d}{\varepsilon_i \cdot \varepsilon_o}\right) \cdot (1 + \lambda \cdot V_{ds}) \cdot \int_{n_{indd}(V_{gs}, V_{ds})}^{n_{inds}(V_{gs})} n_{ind} \cdot \mu_{FET}(n_{ind})\, dn_{ind}$$

$$I_{ds}(V_{gs}, V_{ds}) := if(V_{ds} < V_{On}, 0 \cdot amp, I_O(V_{gs}, V_{ds} - V_{On}))$$

Create a range of drain to source voltages to graph out the current as a function of gate to source voltage. Also read in the data from the measured TFT.

$$VGS := READPRN(TFTVGS_{TXT}) \cdot volt \qquad IGS := READPRN(TFTI\_VGS_{TXT}) \cdot 10^{-9} \cdot amp$$

$$VDS := READPRN(TFTVDS_{TXT}) \cdot volt \qquad IDS := READPRN(TFTI\_VDS_{TXT}) \cdot 10^{-9} \cdot amp$$

$$gs := 0 .. length(VGS) - 1$$

$$ds := 0 .. length(VDS) - 1$$